

# TECHNOLOGY UPDATES AT ELECTRONICA 2024

RENESAS ELECTRONICS CORPORATION

NOVEMBER 13, 2024

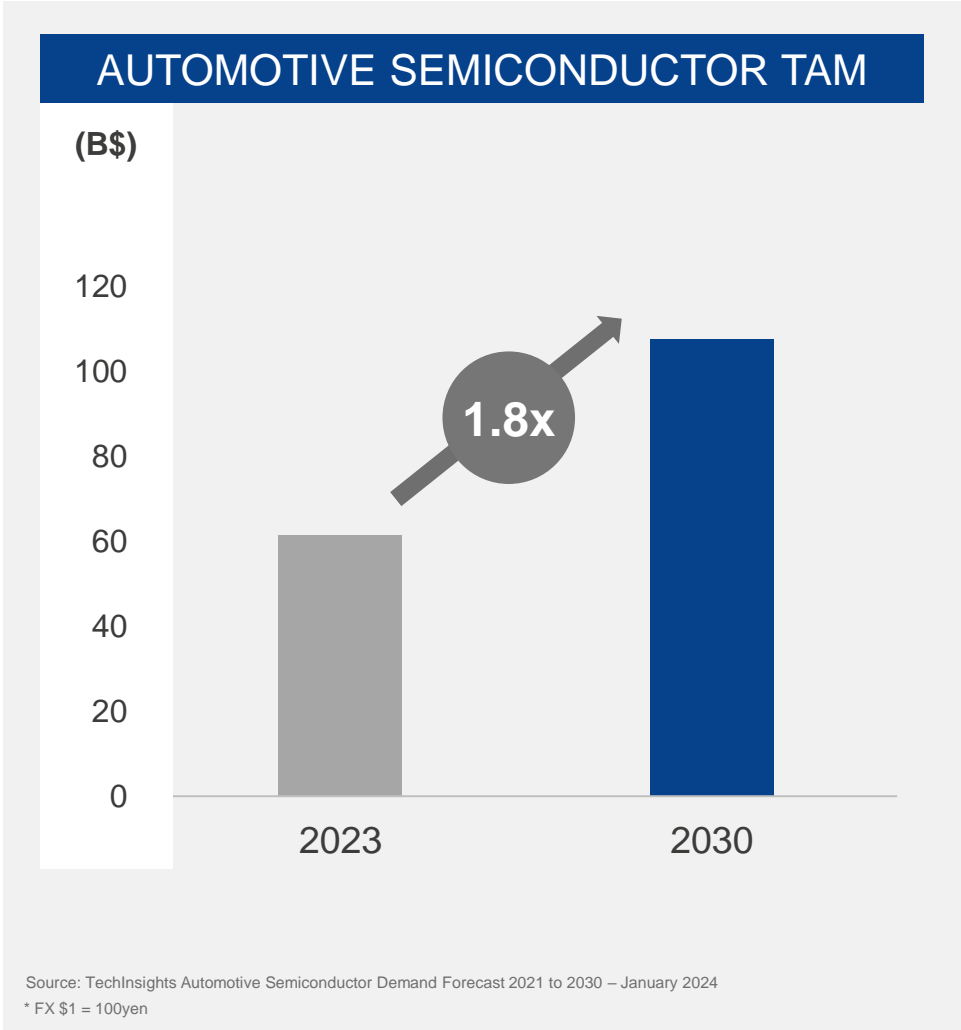
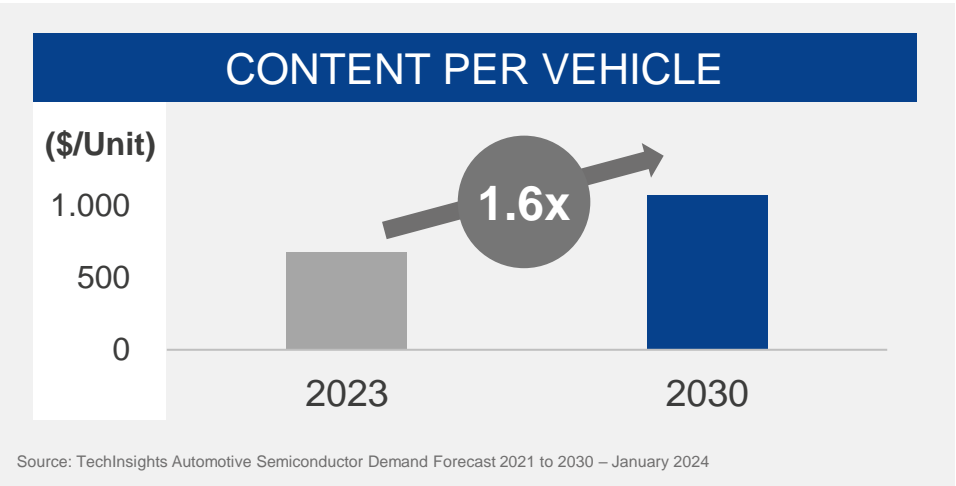
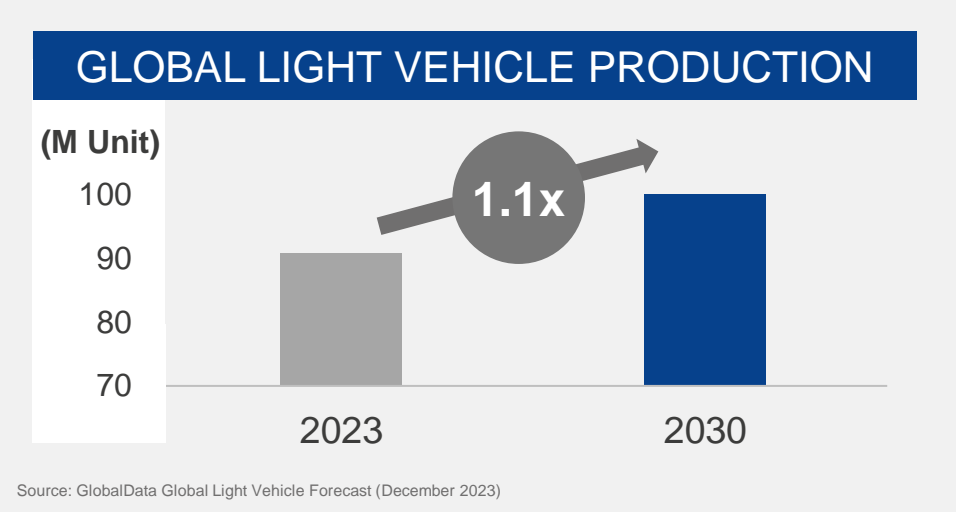
VIVEK BHAN

SVP & GM OF HIGH-PERFORMANCE COMPUTING

RENESAS ELECTRONICS CORPORATION

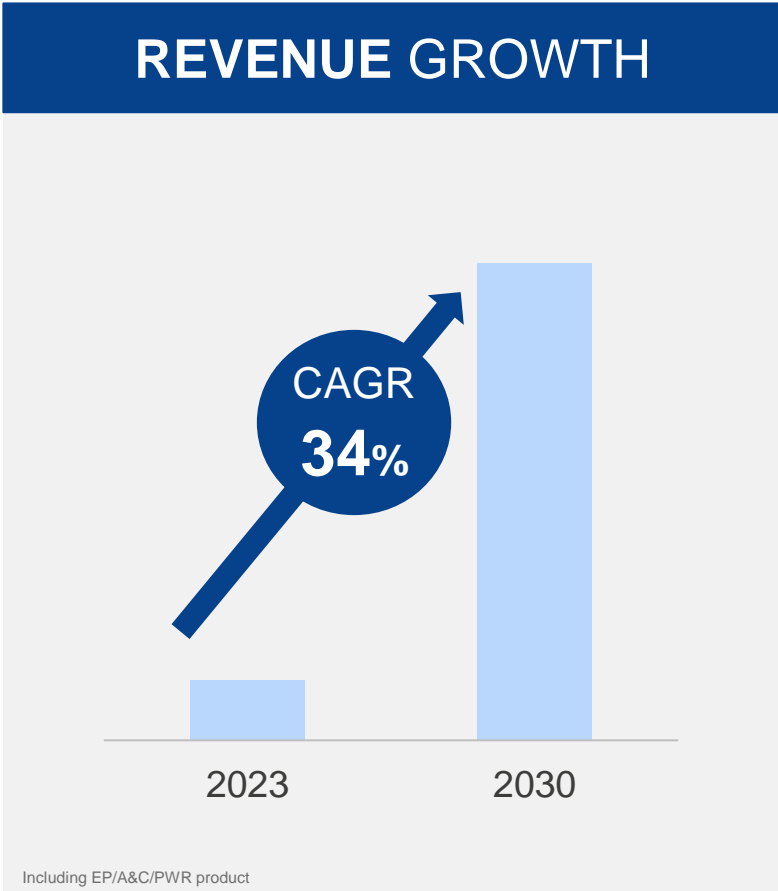
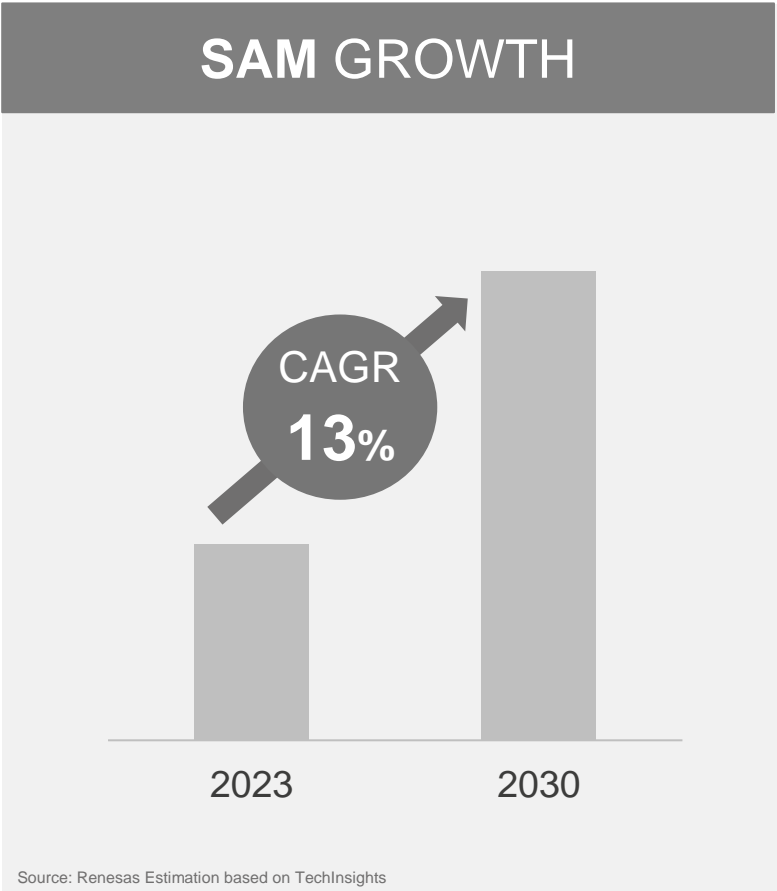
# MARKET OUTLOOK (AUTOMOTIVE)

Auto semiconductor market growth is driven by content per vehicle



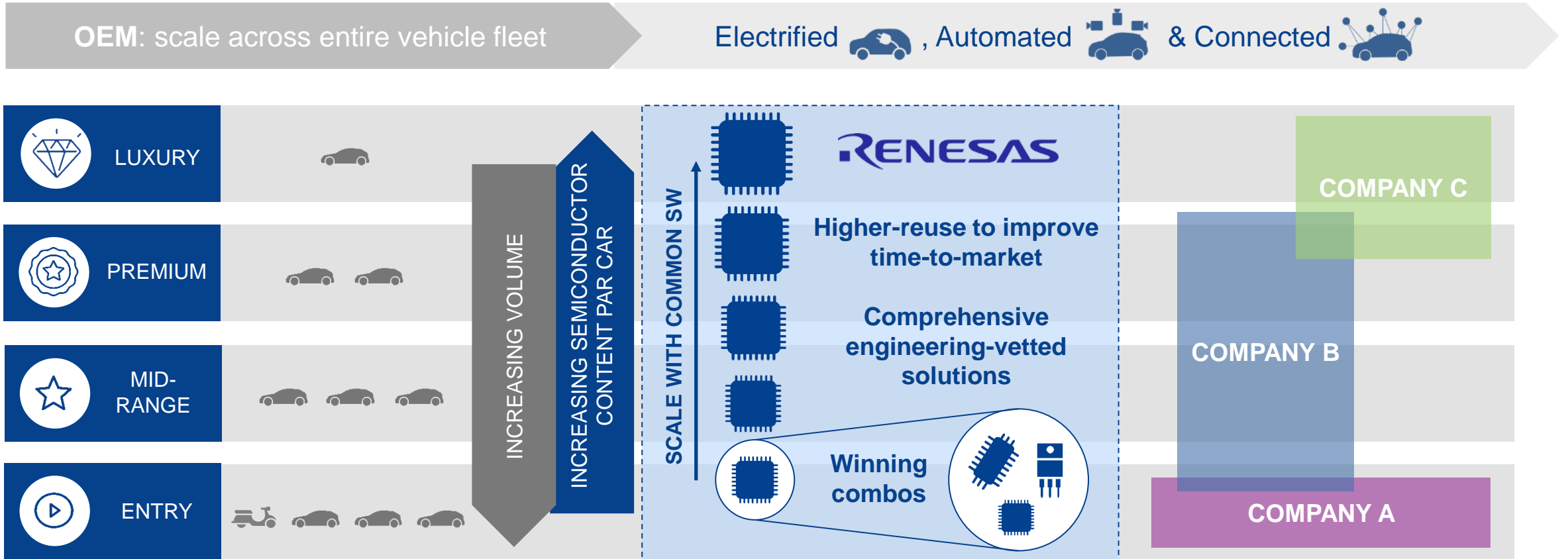
# RENESAS GROWTH IN ADAS MARKET

Revenue growth is expected to outperform the market



# RENESAS AUTOMOTIVE STRATEGY

Full portfolio from MCUs to SoCs with scalable, flexible and customizable platform



A blue wireframe illustration of a car's front and side profile, positioned on a perspective view of a road with lane markings. The entire scene is rendered in a glowing blue color scheme.




# TODAY'S ANNOUNCEMENT

NEXT-GENERATION R-CAR X5H SOC

# AUTOMOTIVE MARKET LANDSCAPE

## ONE SIZE DOES NOT FIT ALL

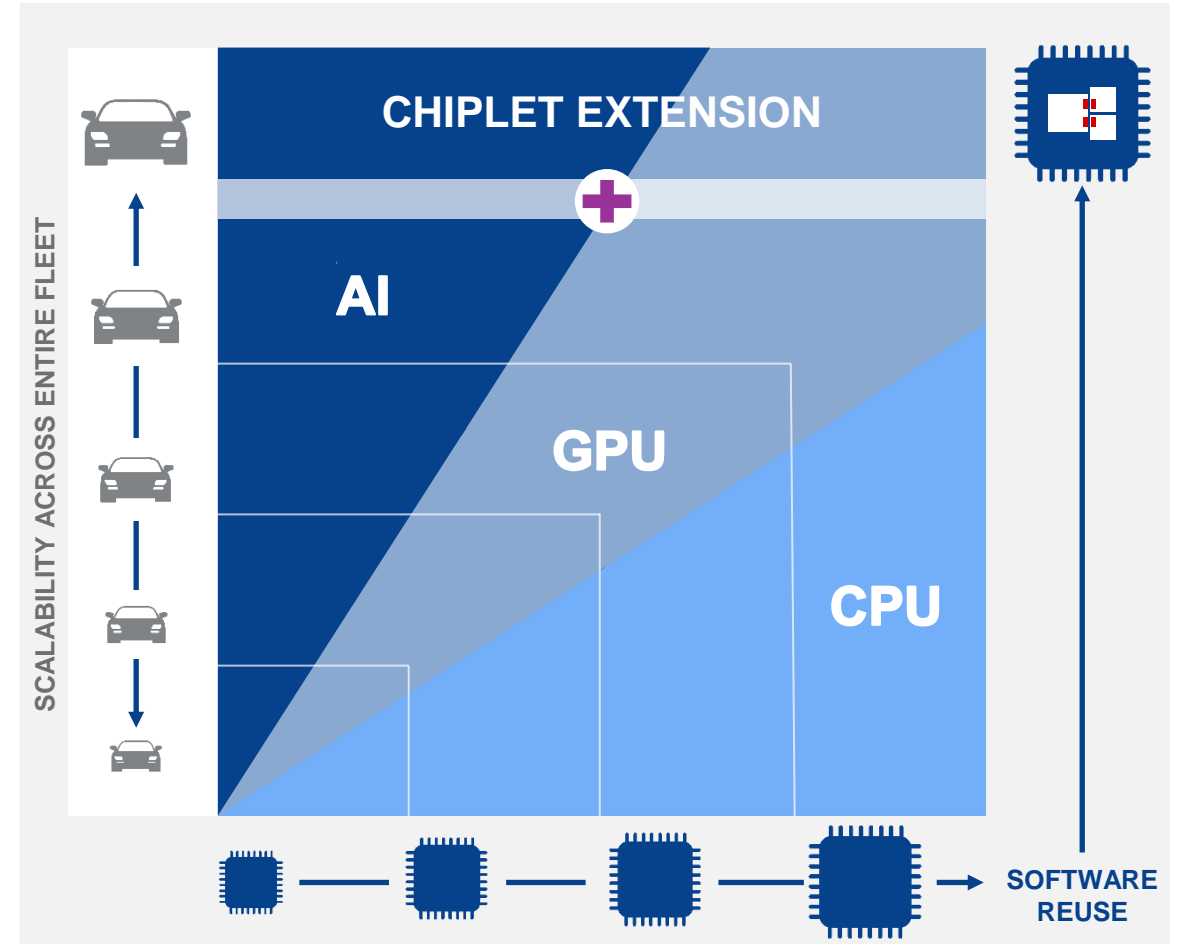
Industry trends are increasing demand for SoC portfolio

-  Mass deployment of advanced ADAS
-  Data and software-oriented E/E architecture
-  Shift to central car compute and domain integration

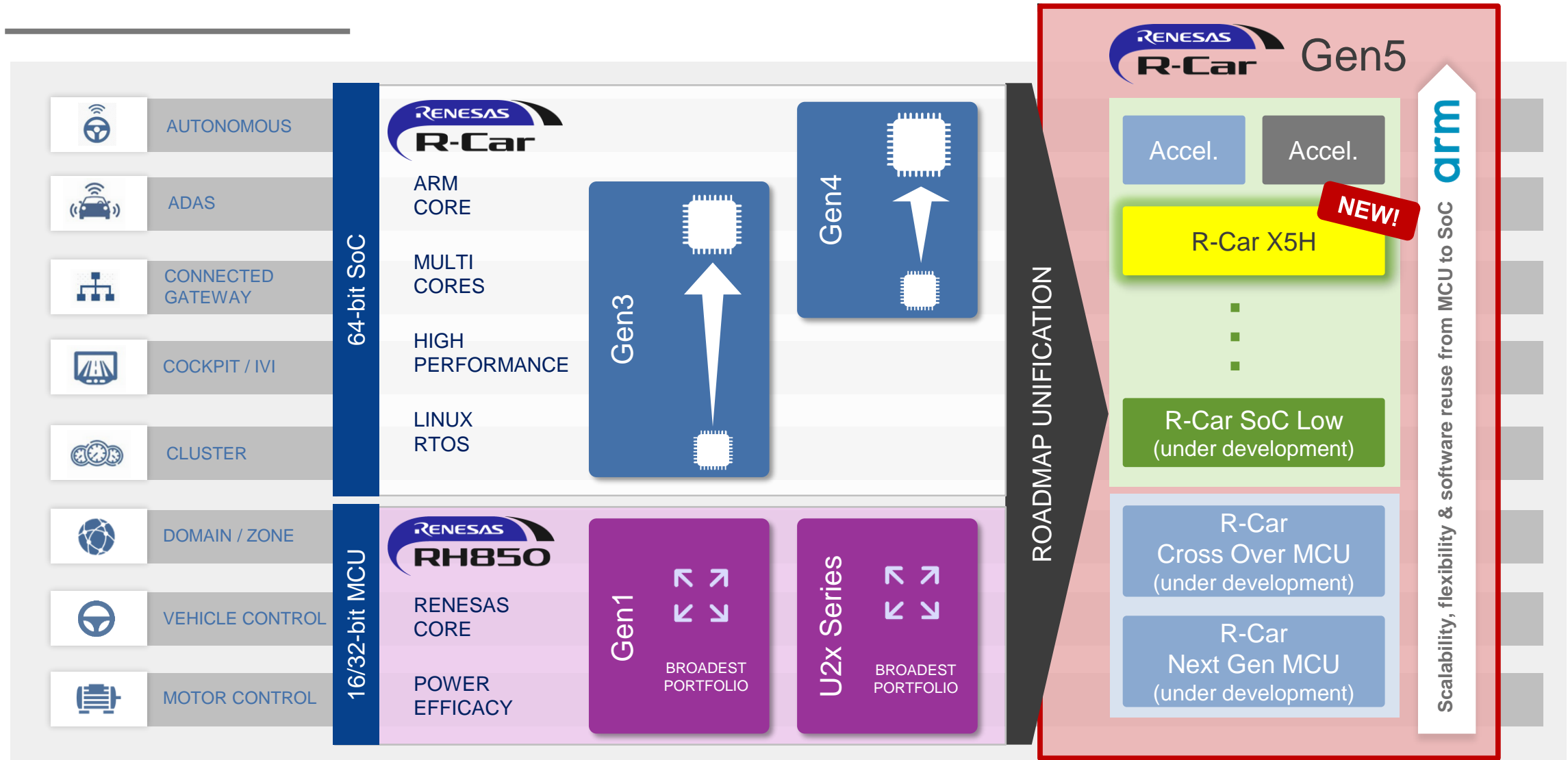
**SoC requirements**

Scale for entire vehicle fleet  
R&D efficiency via software reuse  
Centralized & domain compute

### SCALABLE COMPUTE PLATFORM: MONOLITHIC & MULTI-DIE CHIPLETS

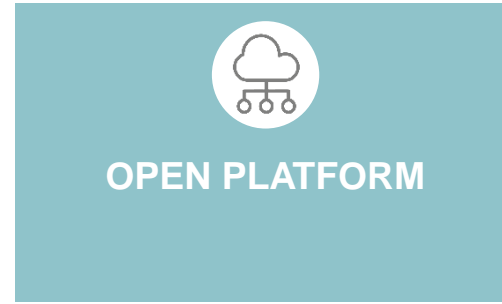
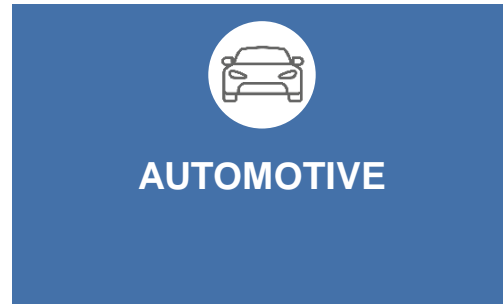
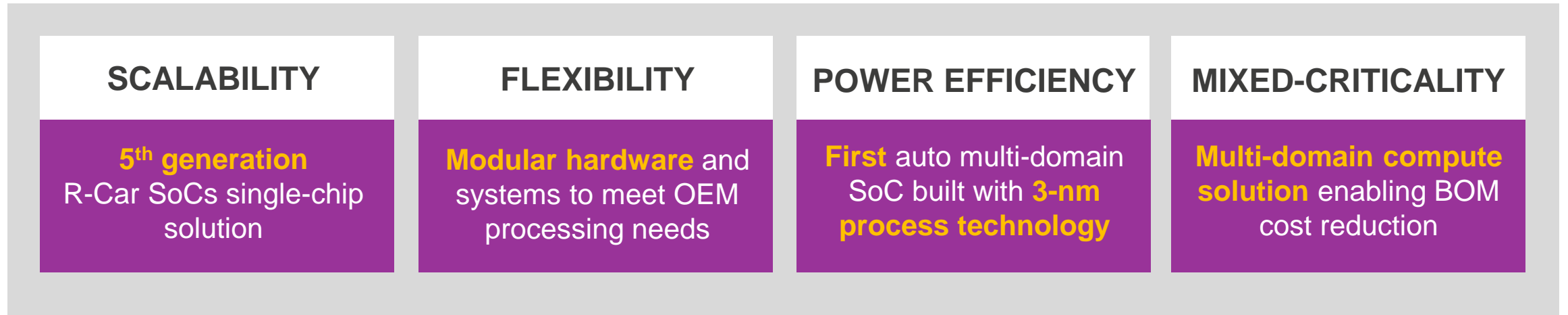


# SCALABLE R-CAR GEN5 SOC & MCU ROADMAP



# ANNOUNCING R-Car X5H

First automotive multi-domain SoC built with **3-nm process technology**





# R-Car X5H SoC: SCALABILITY

Designed to address the shift to centralized architecture

Multi-cluster Arm Cortex-A720AE  
**>1000K DMIPS**, ASIL D support

Multi-stage security arch. featuring  
**dedicated** security accelerator

LPDDR5x supporting over  
**250GB/s** memory throughput

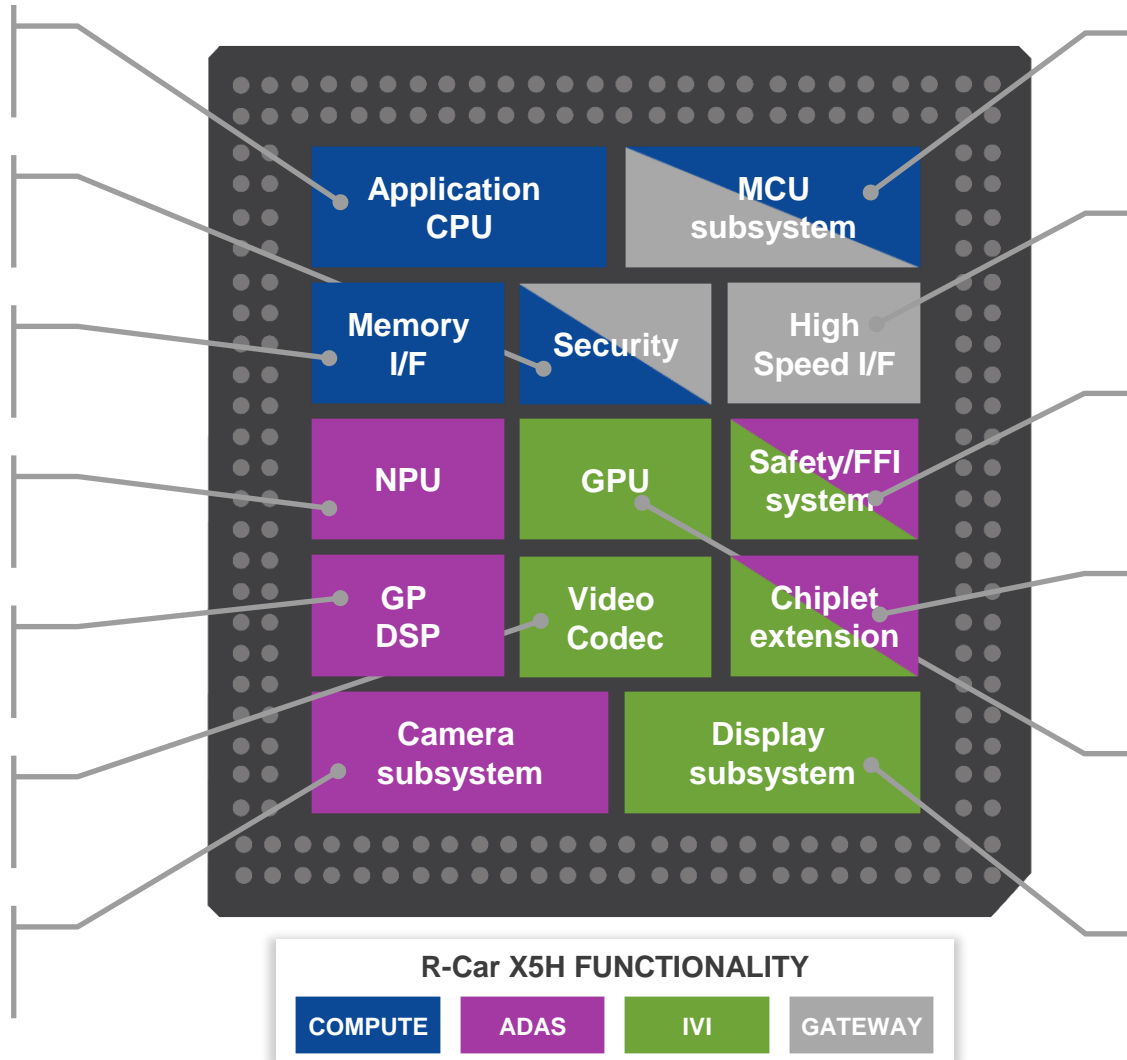
Best-in-class power efficiency AI  
acceleration up to **400 TOPS<sup>(1)</sup>**

Offload NPU & CPU with general  
purpose **DSP cores**

**Multi-4k** media streaming  
supporting H264/5, VP9, and AV1

**Multi-megapixel** camera  
processing with ISP & DOF HWA

<sup>(1)</sup>: Sparse <sup>(2)</sup>: Manhattan 3.0 benchmarking



Arm Cortex-R52 over **60K DMIPS**,  
supporting ASIL B/D & low-power modes.  
**>10MB** on-chip SRAM

High speed interconnects including  
**PCIe Gen4/6**, USB2/3 and 8-port  
**ethernet switch**

**ASIL D** support without ext. MCU. HW-  
supported **FFI for mixed criticality** apps.  
Flexible QoS.

Open architecture / chiplet with  
**standardized UCIe** die to die  
interconnects and APIs

High performance GPU up to **4 TFLOPS**  
**equivalent<sup>(2)</sup>** for leading-edge graphics,  
supporting HW virtualization

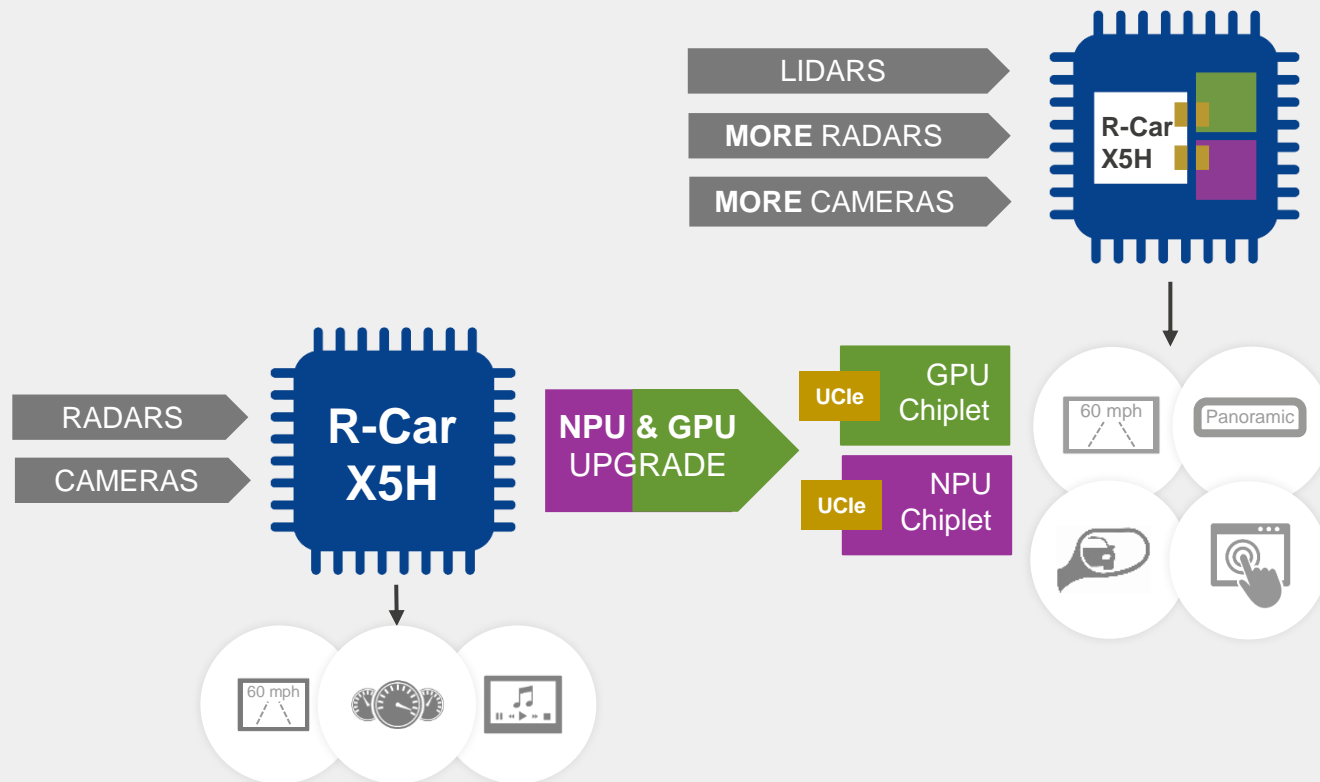
Multistream DisplayPort supporting over  
**10 displays and up to 8k** panoramic  
display

# THE PROBLEM WE ARE SOLVING: FLEXIBILITY

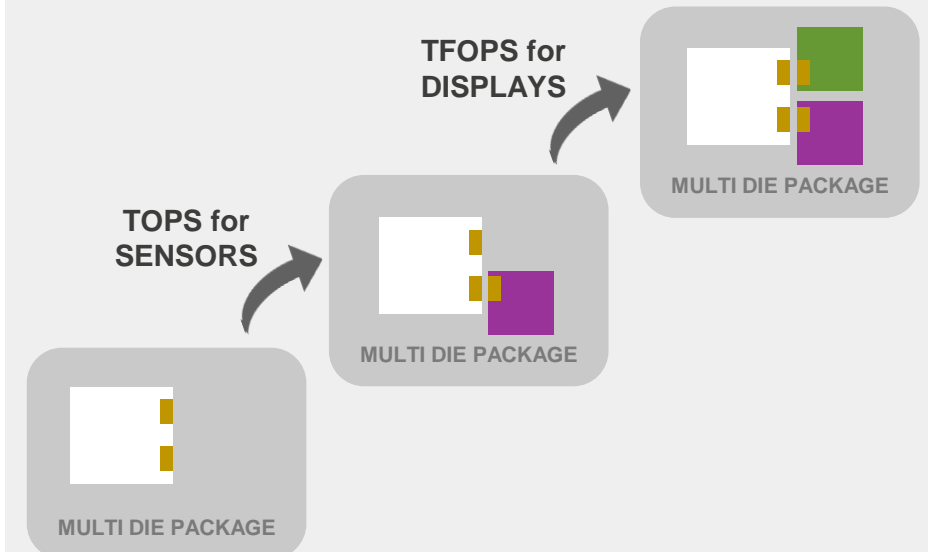
Cost effective multi-domain scalable integrated solutions with **chiplet extension** to scale up

## Combination of NPU and GPU chiplet extension in single SoC package

### MULTI DIE PACKAGE



## Hardware compatibility via SIP option (FCBGA)

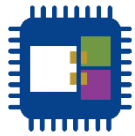


# R-Car X5H SoC WITH INTEROPERABILITY: FLEXIBILITY

Modular hardware and systems to meet OEM processing needs



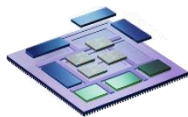
Integrates the standard UCle (Universal Chiplet Interconnect Express) die-to-die interconnect and APIs



Facilitates interoperability with other components in a multi-die system



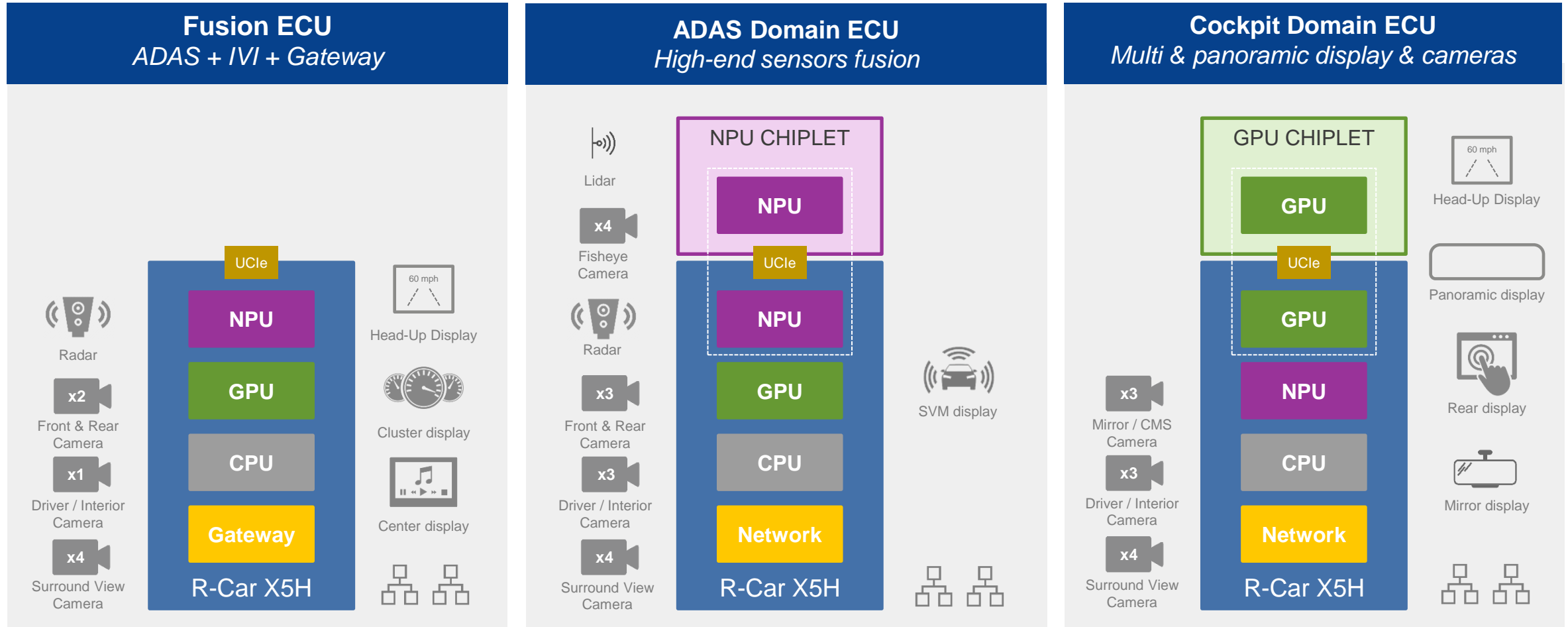
Mix and match different functions and customize systems including future upgrades across vehicle platforms



Different flavor of packaging options supported enabling an open ecosystem for on-package innovation

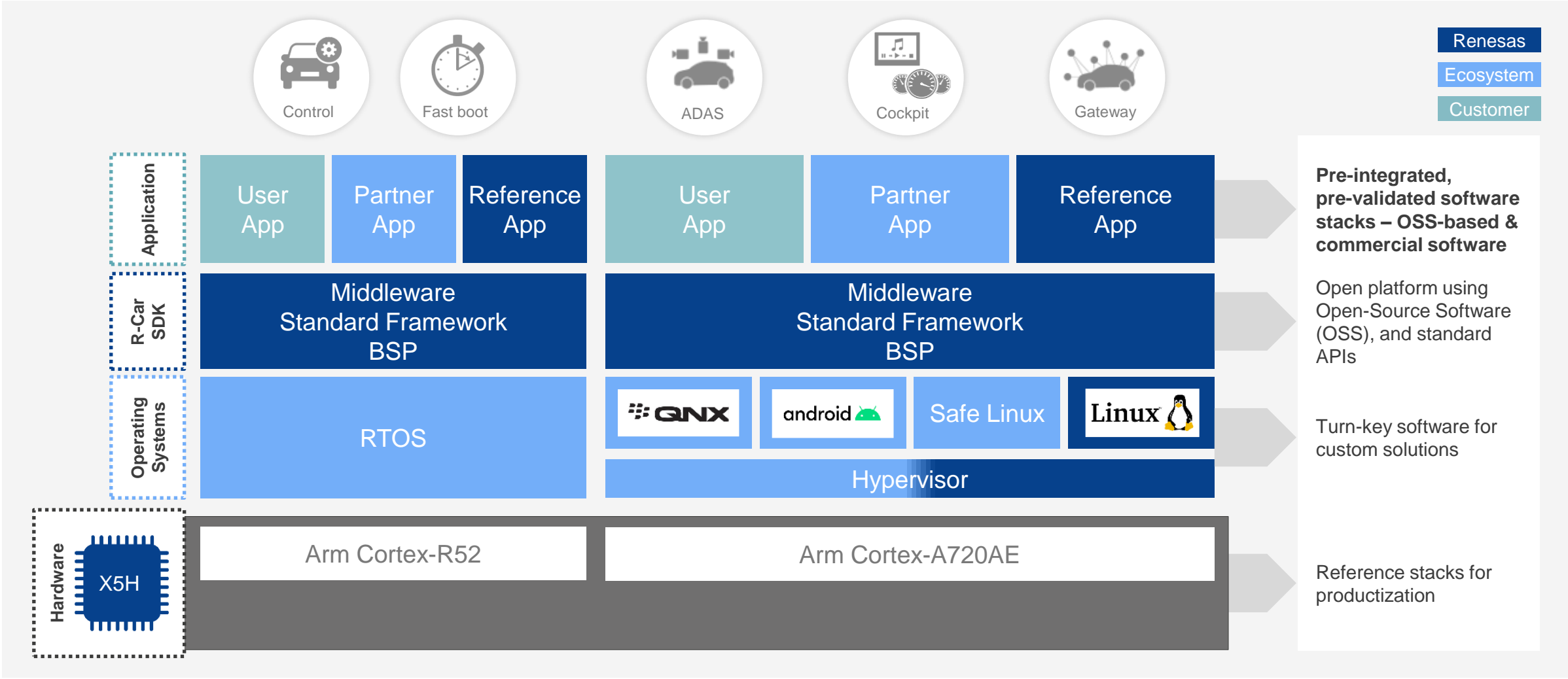
# R-Car X5H SoC USE CASES: FLEXIBILITY

Modular hardware and systems to meet OEM processing needs



# R-Car X5H SoC DEVELOPMENT ENVIRONMENT: FLEXIBILITY

Maximize reuse of development assets with R-Car Open Access (RoX) SDV platform

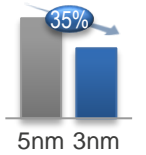


# R-Car X5H SoC IN MONOLITHIC DESIGN: POWER-EFFICIENCY

Industry-first 3-nm multi-domain central car computer with optimized power design



Industry-first 3-nm automotive qualified multi-domain central car computer



30-35% improvement in power efficiency for specific workloads compared to the next higher node

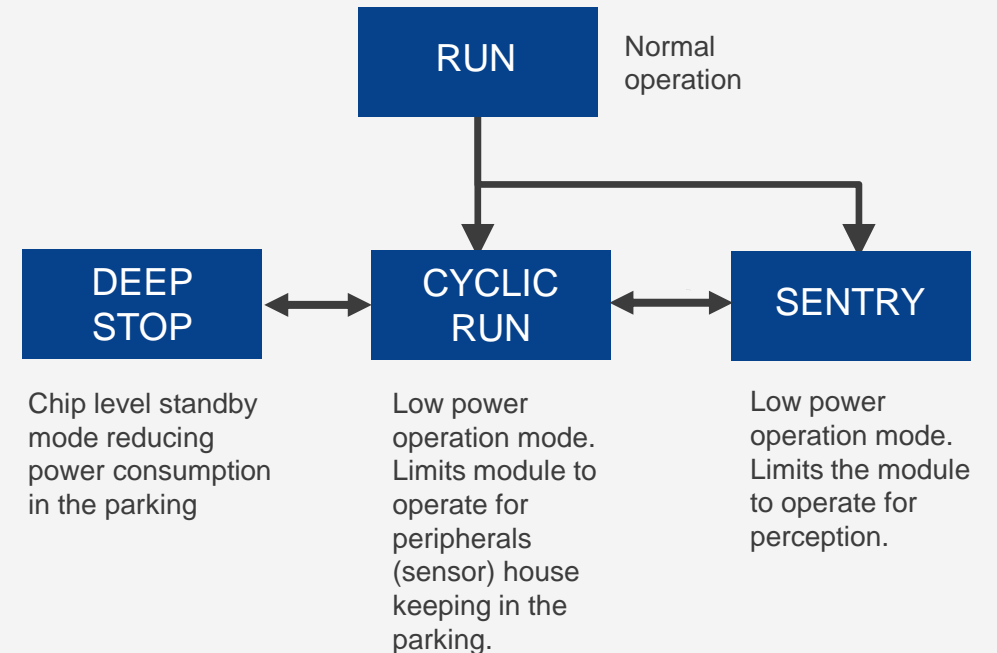


Integrates AI processing for 360-degree perception with highly efficient TOPS/Watts



Best-in-class power, non liquid cooled\* safety compliant central car computer

Optimized power design and power modes to support modern automotive use cases

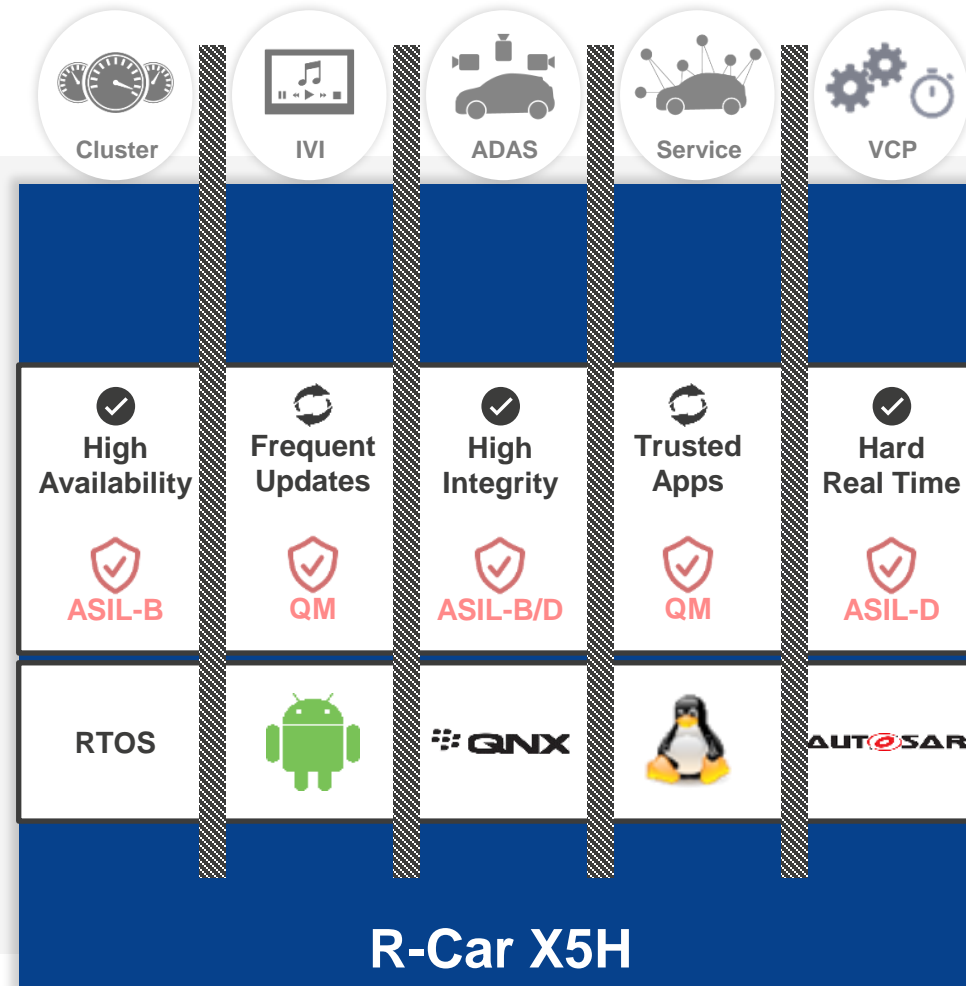


(\*): Specific use case conditions

# R-Car X5H SoC: MIX-CRITICALITY

Multi-domain compute solution enabling BOM cost reduction

- Hosting multiple compute domains (aka X-domain) in a single SoC requires to guarantee their respective specificities
- Software methods alone like hypervisor can't guarantee full freedom from interference
- Hardware measures are needed



R-Car unique & industry proven freedom from interference (FFI) solution extended to R-Car Gen5

Ensure domain isolation via deep hardware measures on R-Car X5H including RegionID, memory protection by RegionID or QoS extension

# R-Car X5H SoC

First automotive multi-domain SoC built with 3-nm process technology



## DESIGNED TO ADDRESS THE SHIFT TO CENTRALIZED ARCHITECTURE



- **Scalable:** 5th generation R-Car SoCs single-chip solution
- **Flexible:** Modular hardware & systems to meet OEM processing needs
- **Power-efficient:** First multi-domain SoC built with 3-nm process technology
- **Mix-criticality:** Multi-domain compute solution enabling BOM cost reduction



- **Development start:** Today with RoX Virtual Platform (“shift-left”)
- **Silicon:** Sampling to select automotive customers in 1H/2025
- **Production:** Scheduled in 2H/2027



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[Renesas.com](https://www.renesas.com)