Presentation Highlights: A 65nm Silicon-on-Thin-Box (SOTB) Embedded 2T-MONOS Flash – 2019 Symposia on VLSI Technology and Circuits

Low-Power SOTB™-Based Technology for Embedded Flash Memory Enables Energy Harvesting and Eliminates Need for Batteries

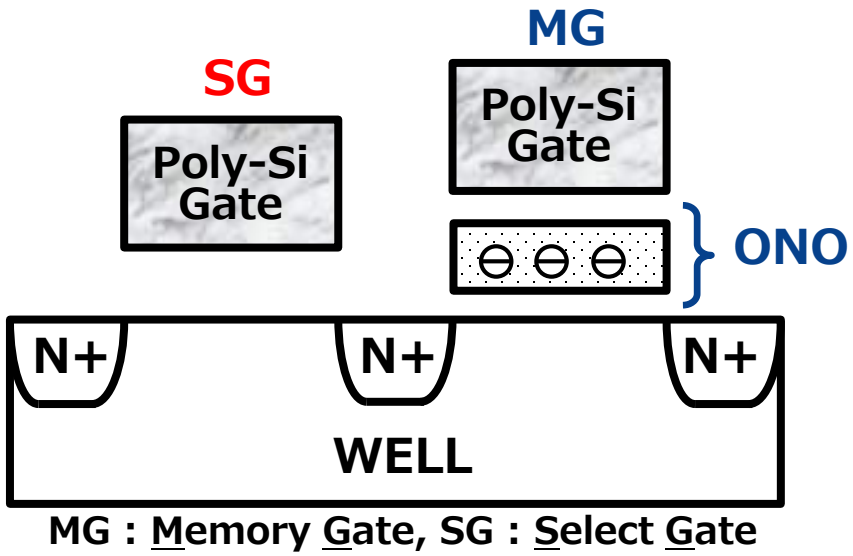
Key Features of the Newly Developed Technology

- Low-power 2T-MONOS flash memory ideally suited to the SOTB process
- Sense amplifier circuit and regulator circuit technology for ultra-low energy consumption
- Circuit technology that dramatically cuts data transfer energy consumption

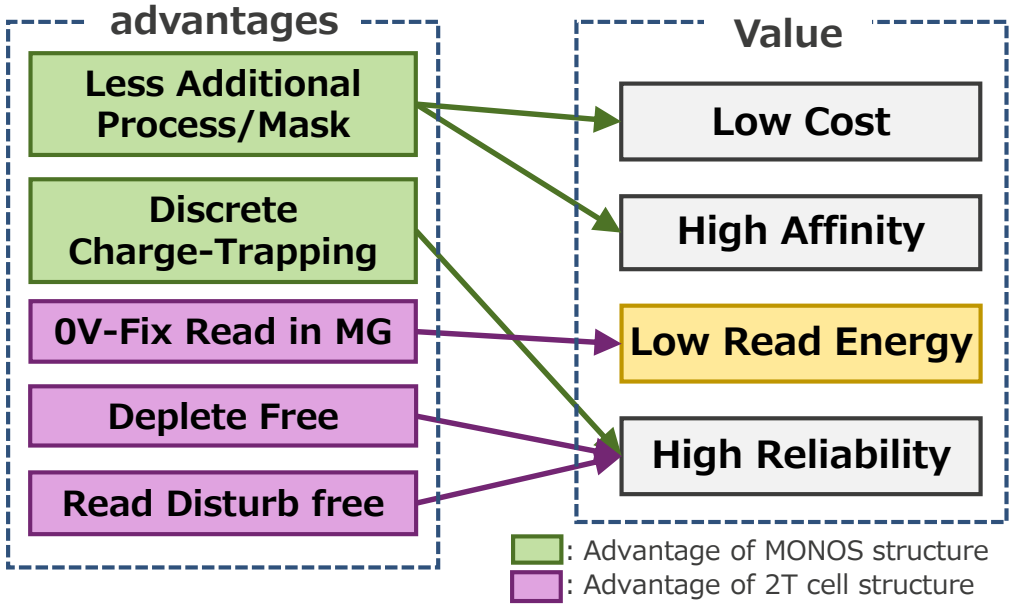
Circuit Technique: Low-Power 2T-MONOS Flash Memory Ideally Suited to the SOTB Process

The 2T-MONOS flash memory using the SOTB process has the advantages of both a two-transistor structure and a discrete charge-trapping structure, achieving low cost, high reliability, and **low energy consumption read operation suitable for energy harvesting.**

Memory gate and select gate of 2T-MONOS

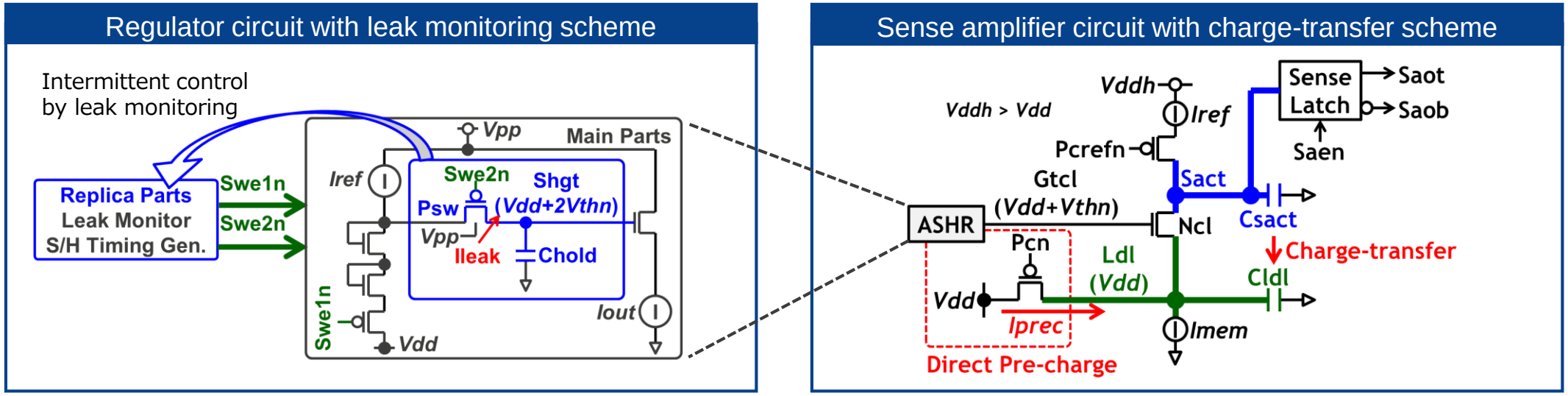


Advantages and value



Circuit Technique: Sense Amplifier and Regulator Circuit Technologies for Ultra-Low Energy Consumption

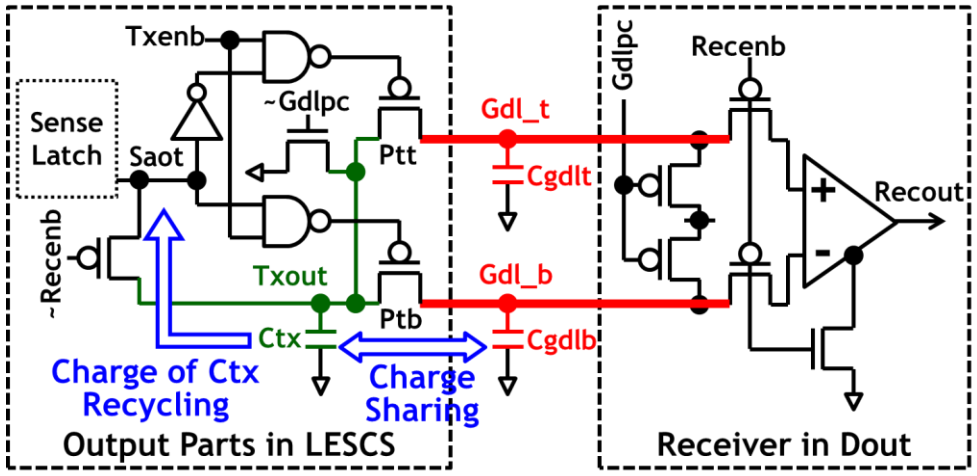
- To reduce the read energy of flash memory, it is necessary to reduce the sensing operation's energy consumption, as this occupies most of the read operation.
- Renesas developed a) A **single-ended sense amplifier circuit technology** applies a new charge transfer scheme to improve pre-charge speed and energy efficiency, and b) a **regulator circuit technology** that applies leak monitoring to perform optimal intermittent control of the sense amplifier's reference voltage, which consumes energy in a constant manner. As a result, Renesas achieved a **29% reduction in read energy reduction.**



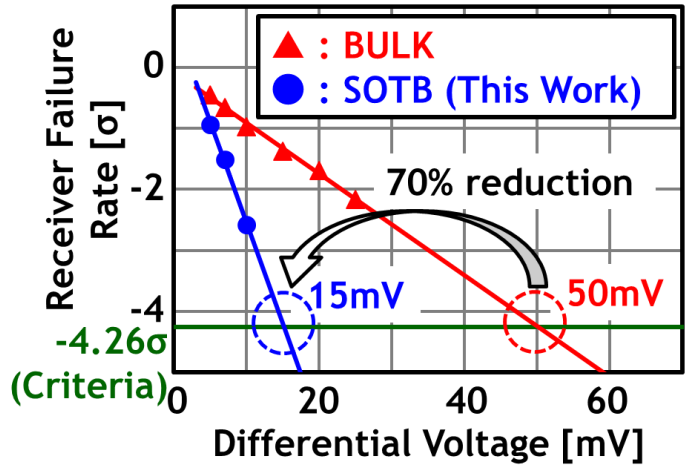
Circuit Technique: Dramatically Reduced Transmission Energy Consumption

- Data transmission operation is another key for further read energy reduction.
- One characteristic of the SOTB process is minimal variation in the transistor threshold (Vth), and the newly developed **data transmission circuit technology** takes advantage of this to achieve data transmission with extremely small voltage amplitude. As a result, Renesas achieved a **30% reduction in read energy**.

Data transmission circuit with small voltage amplitude

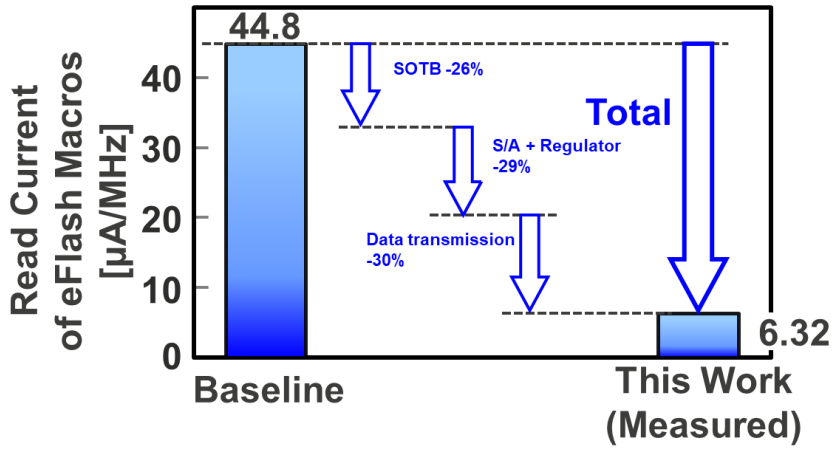


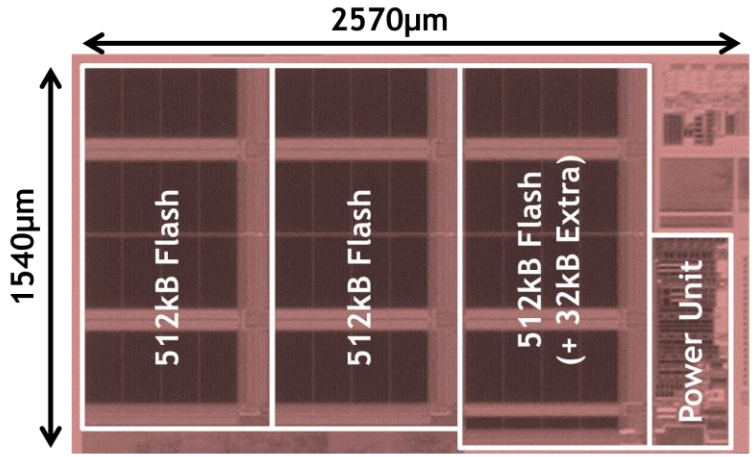
Small amplitude effect by SOTB



Criteria is calculated from chip failure rate < 0.1%

Developed Embedded Flash Macro Features





	This work
Technology	65nm SOTB 2T MONOS
Memory Capacity	1.5MB
Core Voltage	0.75 V
Read Energy	**0.22pJ/bit**
Read Current (32bit Bus)	**6.32μA/MHz**
Read Frequency	**64MHz**
Endurance	**1M Cycles**