EMBEDDED TARGET FOR RH850 MULTICORE

JUNE 14, 2018
AUTOMOTIVE SOLUTION BUSINESS UNIT
SHARED R&D DIVISION 1

RENESAS V-MODEL SOFTWARE DEVELOPMENT SOLUTIONS

Model-based tool(MBD) and Virtual platform(VPF) is a prototyping tool in the earlier stages

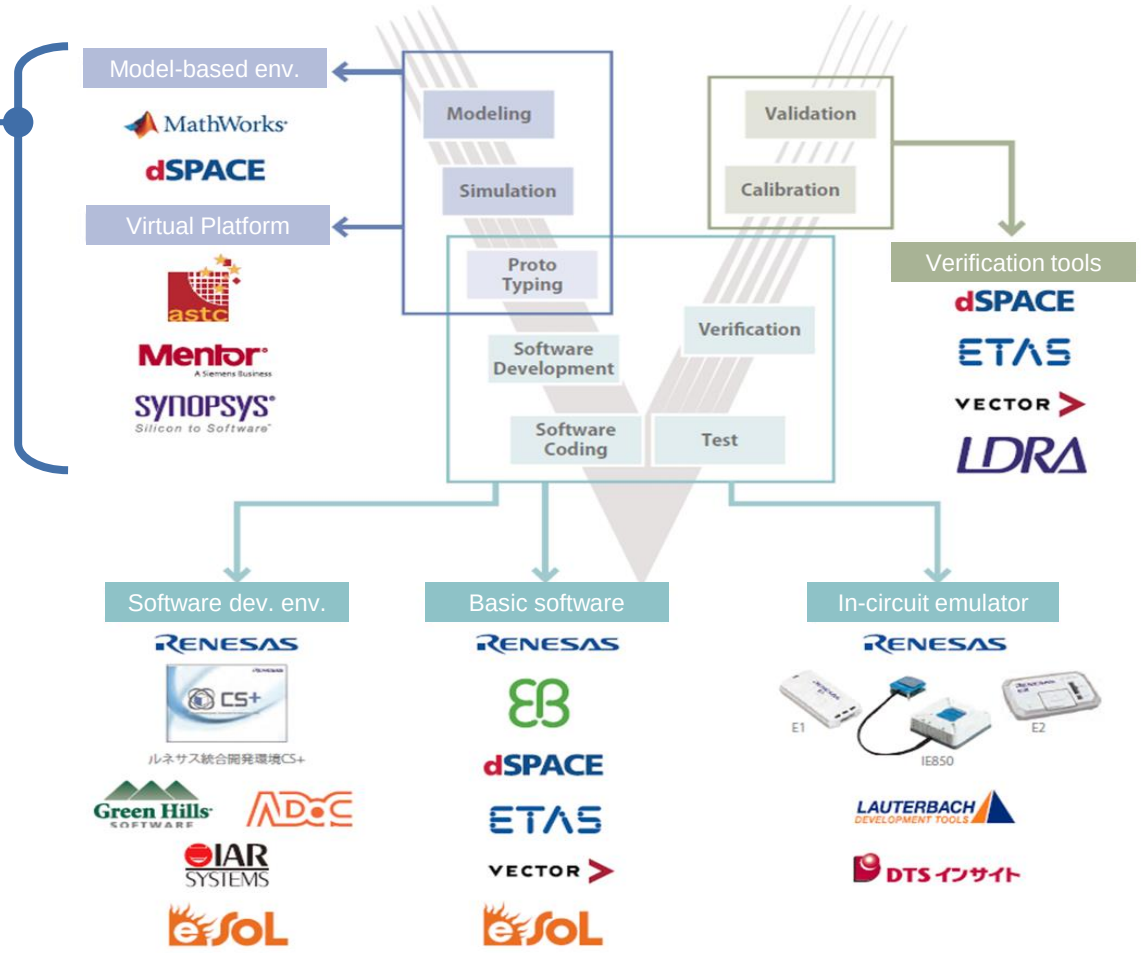
- No implemented software
- No implemented MCUs

Customer Expectation

The customer wants to verify at an early stage from various perspectives to see whether the final system will be established.

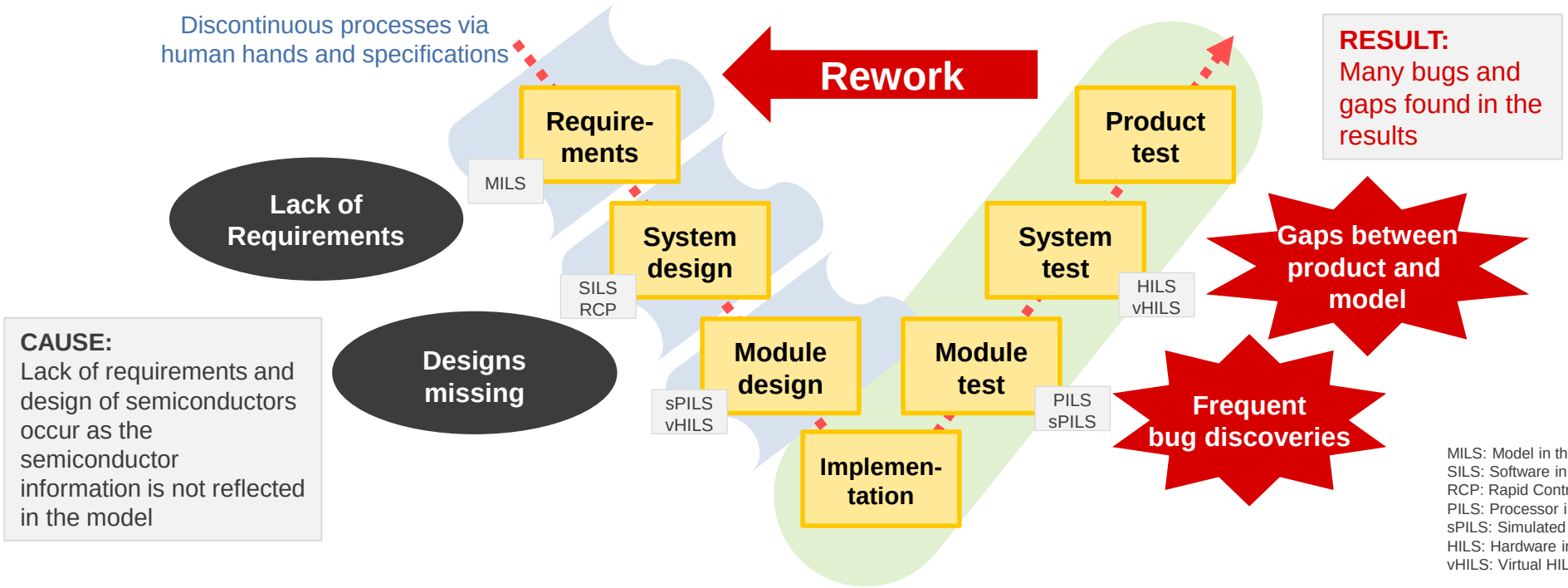
Example Aspects:
- Measure execution performance of algorithm
- Validation system function
- Accelerate software development

etc...



ISSUES REGARDING V-MODEL FOR MANUFACTURING

On the left side of the V-model, information on semiconductor assets are not used. Therefore frequent bugs and gaps will be discovered on the right side of the V-model



→ **For software development as an example, problems found after implementation where execution performance could not be achieved**

BACKGROUND OF SOFTWARE DESIGN FOR COMPLEX PRODUCTS

Increased demands of MCUs for large-scale software

→ **Necessity of multicore MCUs and efficient software development environment**

Smartphone:

12M lines

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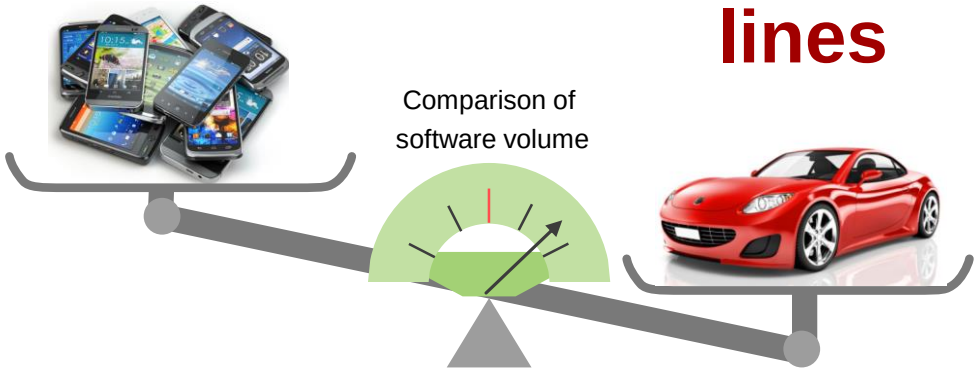
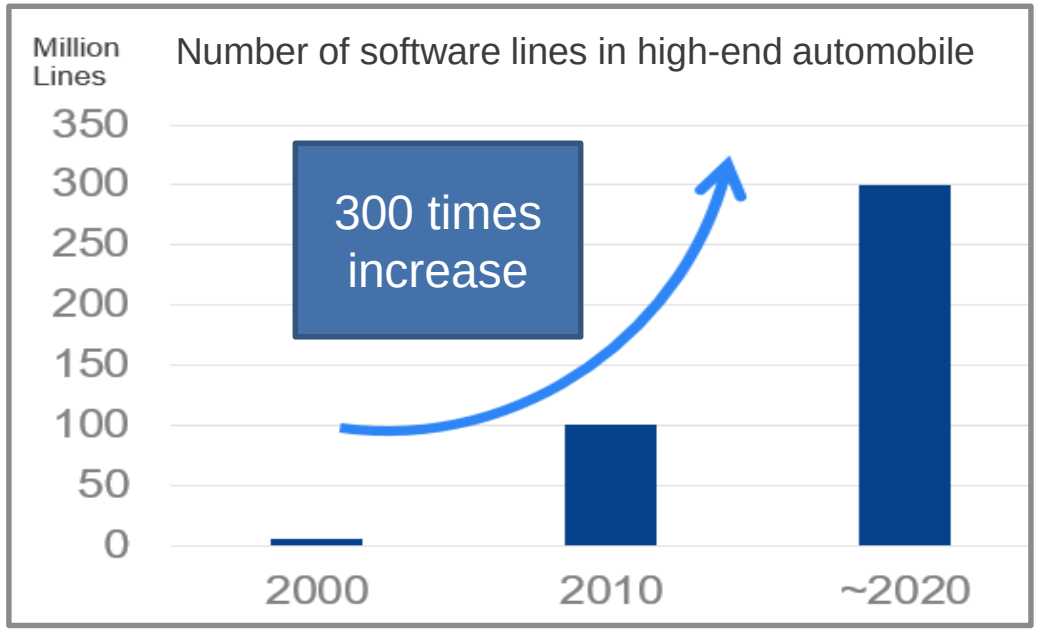
High-end automobile:

Over 100M lines



Comparison of software volume

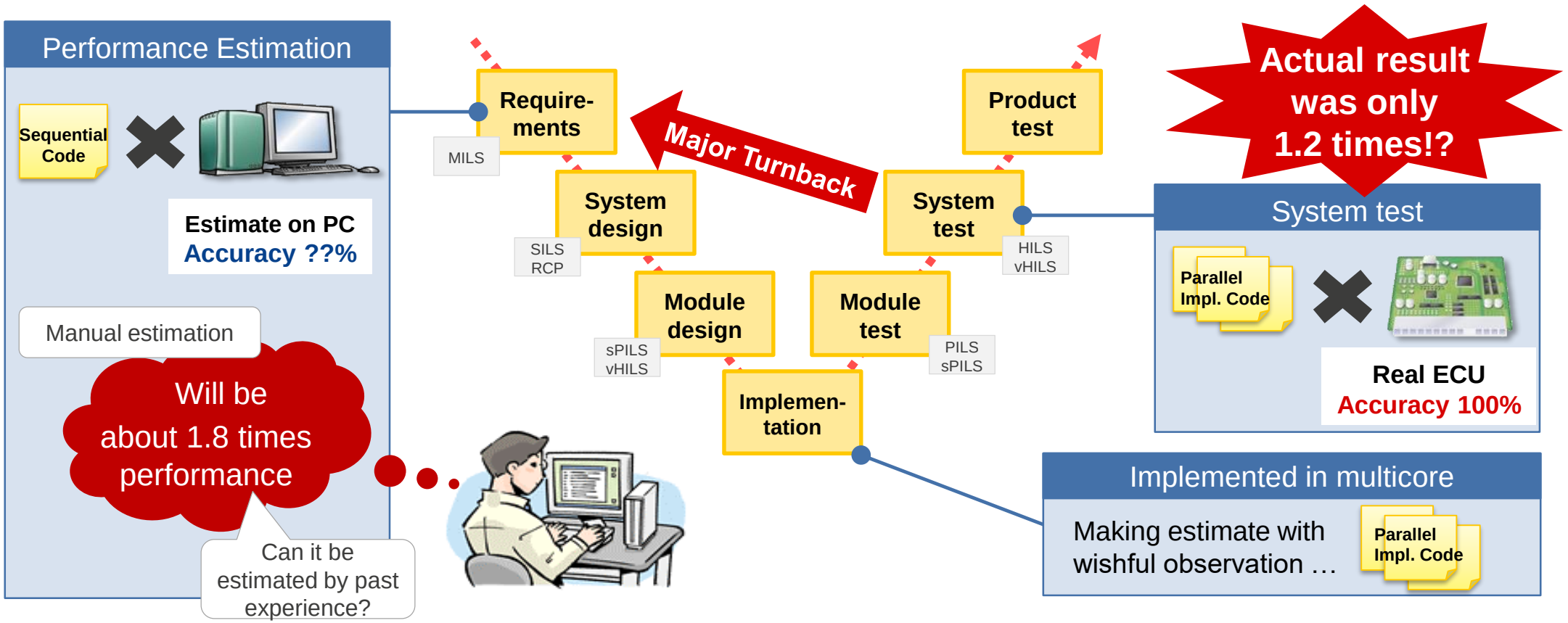
Example of automotive software volume:
Software volume for a high-end automobile is around **8 times** that of a smartphone.
This is expected to increase with the rise of automatic driving.



Source : New York times/IEE

ISSUES OF CONVENTIONAL MULTICORE SOFTWARE DEVELOPMENT

Method up to now could not obtain correct multicore function estimate



HOW TO ESTIMATE MULTICORE SOFTWARE PERFORMANCE

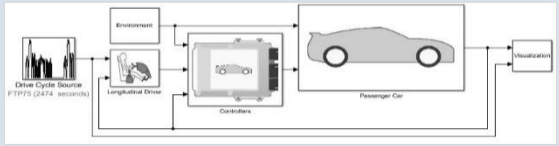
In order for customer design teams to come up with a accurate estimate it takes lots of time and knowledge. These include knowledge of the system, software, semiconductor and 3rd party tools usage.

Knowledge of various fields required

Very difficult to conduct manually

System Behavior

Input scenario | Parameters



MathWorks Powertrain Blockset™

Characteristic of Application

Control parallelism | Data parallelism

Amdahl's law

$$Speedup = \frac{1}{\frac{F}{1} + \frac{1-F}{N}}$$

F: Ratio of sequential execution
N: # of Execution resource ≒ # of CPU

Characteristic of Hardware

Performance of CPU? Number of CPU?

MCU: CPU | CPU | Interconnect | Memory

Interference? Collisions?

Enough memory structure, Band-width, memory size?

Critical path

Load balance

Communication cost

Correct estimation of multicore software by Renesas

SOLUTIONS TO SOLVE ISSUES OF MULTICORE SW DEVELOPMENT

Solution Requirements

Co-simulation with MBD tools(MATLAB/Simulink)	Automatic assignment plan by Model-based parallelization tool	Automatic generation of multicore code for target MCU	Detailed analysis environment by high accuracy MCU simulator
Consideration of system behavior including outside MCU can be clarified	Users can generate and execute multicore software from models without difficult tool setup and without being conscious of software implementation		Be able to evaluate the actual operation on multicore MCUs

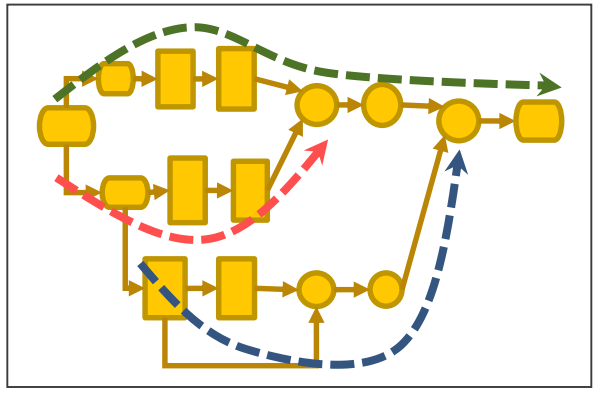
Strong support for multicore software design with MBD

“Renesas Embedded Target for RH850 multicore”

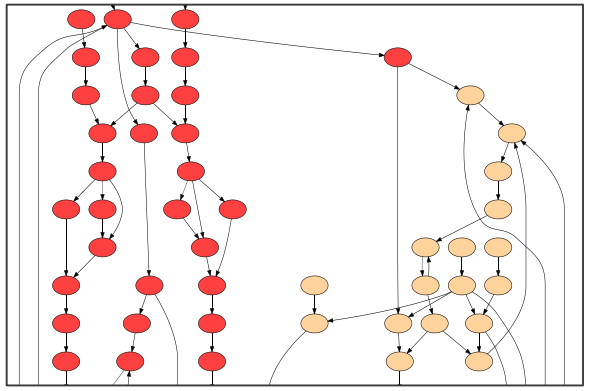
TECHNOLOGY: MODEL-BASE AUTOMATIC PARALLELIZATION

Automatic parallelization based on dependency on model and execution time on microcontroller

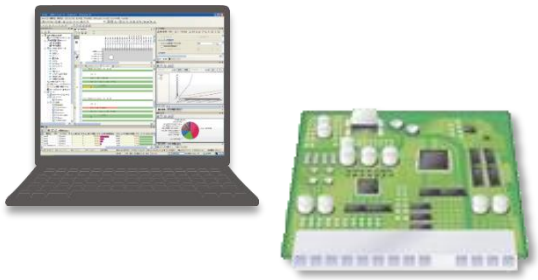
Simulink® Model



Multicore assignment



MCU device information
(Simulator or real-device)



Extraction of parallelism between blocks

Optimal parallelization

Acquire exact execution time of the block

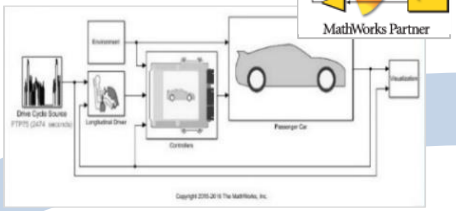
RH850 MULTICORE MODEL-BASE DEVELOPMENT ENVIRONMENT

COLLABORATION OF EMBEDDED TARGET FOR RH850 MULTICORE AND eSOL eMBP

Modeling

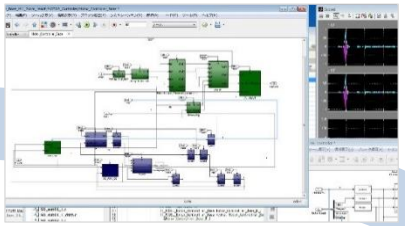
User

MathWorks
MATLAB/Simulink

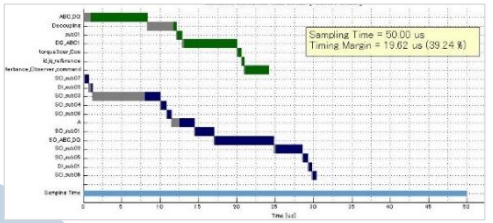


MathWorks Powertrain Blockset™

Result analysis



Model for multicore



Execution profile on multicore

Embedded Target for RH850 Multicore

Full automation of estimate code implementation

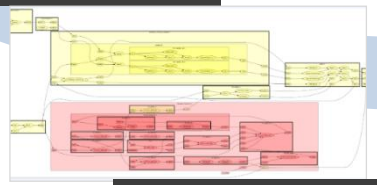
Block performance analysis

IDE

CS+

Measure each block performance by cycle accuracy simulator or real MCU

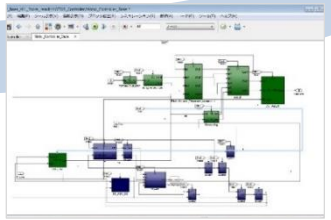
Model structure analysis



Assign to multicore

eMBP **eSOL model-base parallelization**

Transformation to model for multicore



Generation of multicore code & Co-simulation

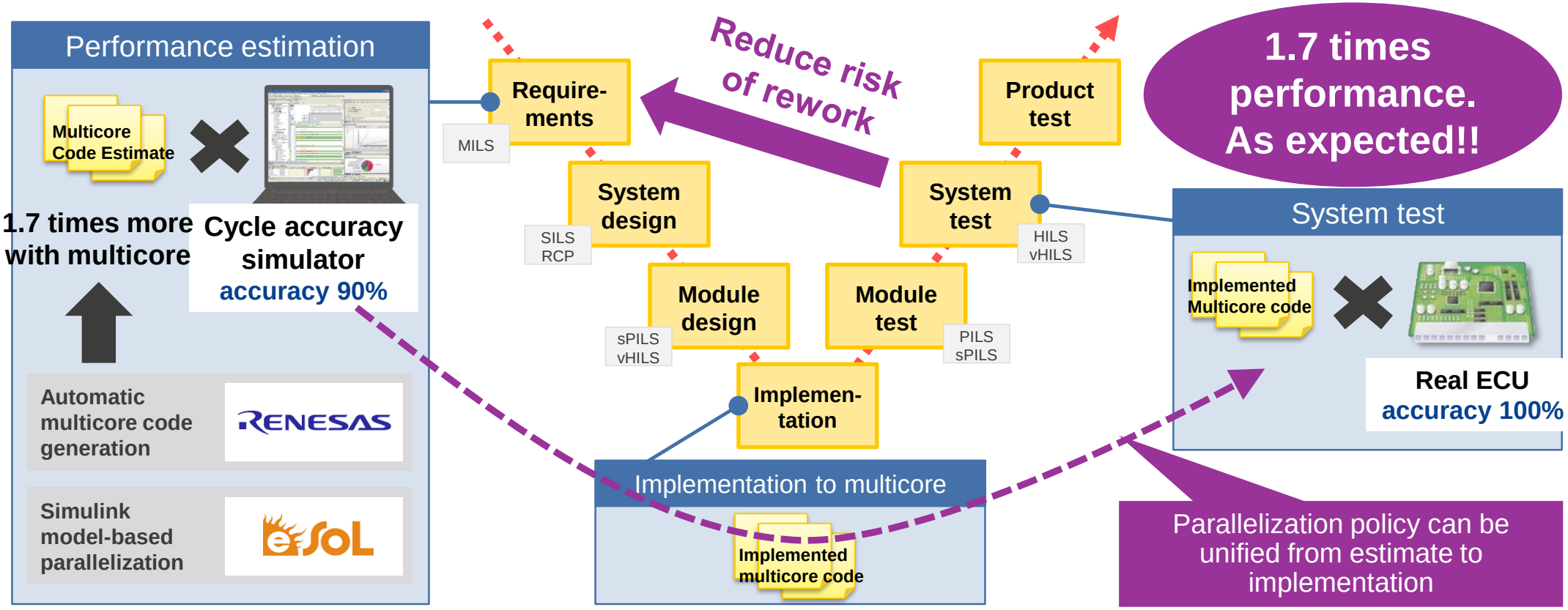
IDE

CS+

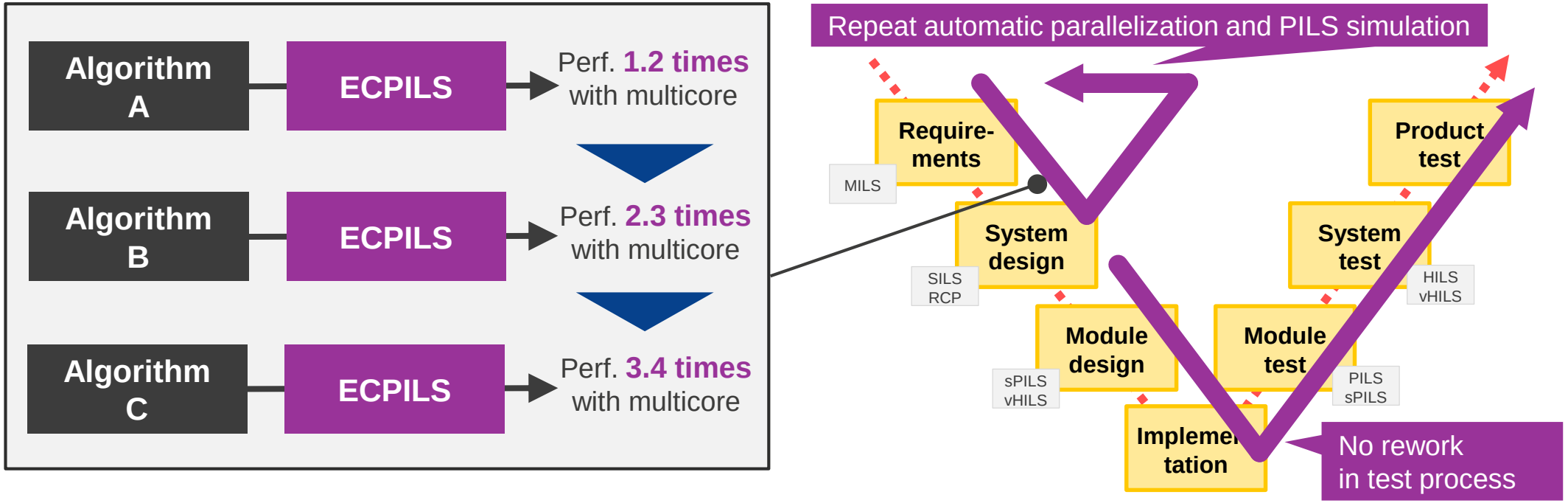
Measure multicore execution profile by cycle accuracy simulator or real MCU

EFFECTS OF MULTICORE MBD ENVIRONMENT

Acquire accurate estimate based on MCU information with multicore MBD environment : Reduce risk of rework



EXAMPLE OF MULTICORE MODEL-BASED ENVIRONMENT



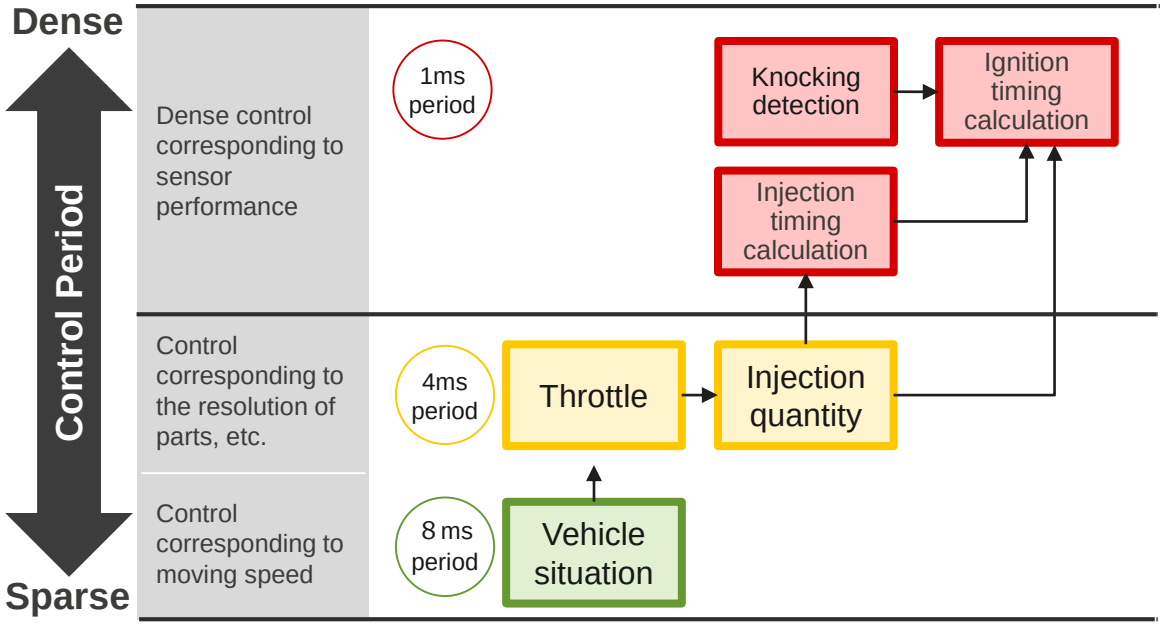
- Build multicore performance at the early stage of V model

→ Proposal of new multicore development process

NEW TECHNOLOGY: SUPPORT FOR MULTIRATE

MULTICORE OPERATION OF MULTIRATE CONTROL FOR ENGINES

Example of Multirate Control for Engine



Automatically schedule various controls with varying periods to CPU1 and CPU2

Example of the Visualization of Multicore Execution

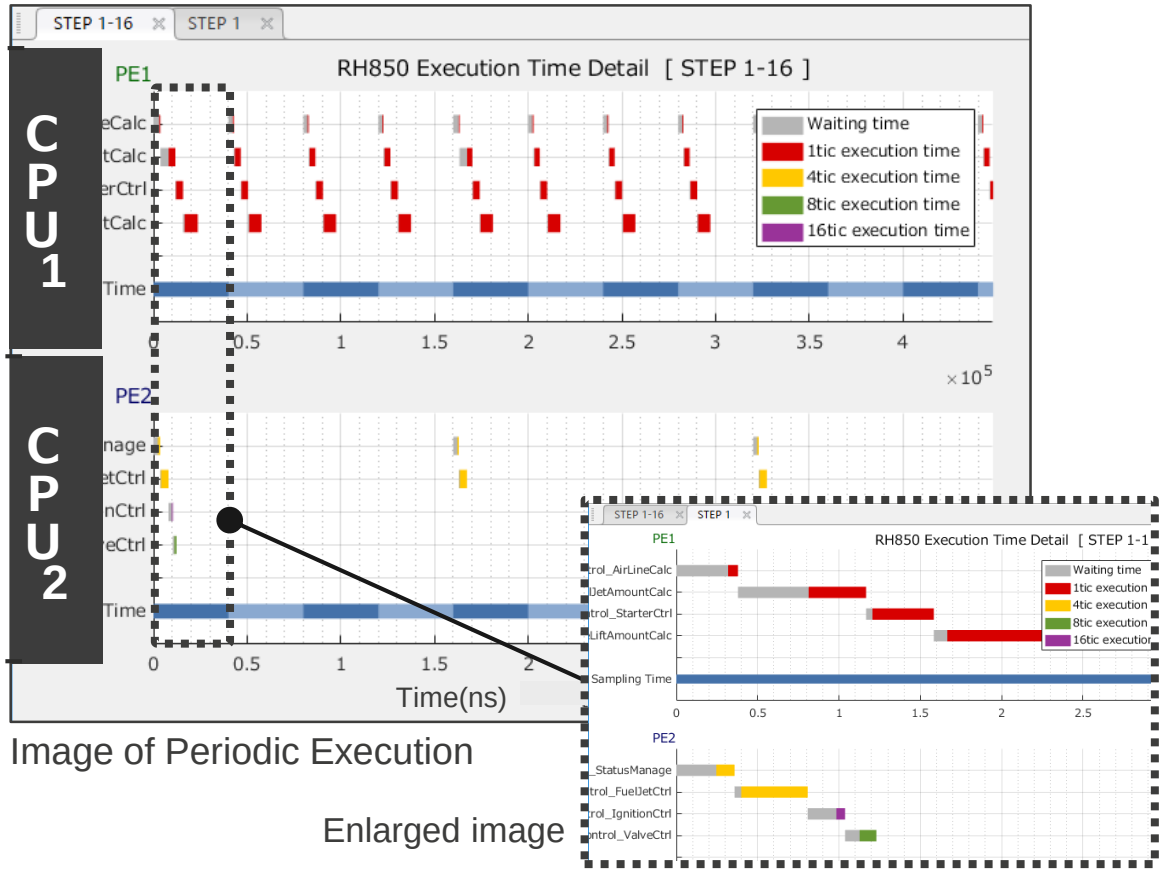
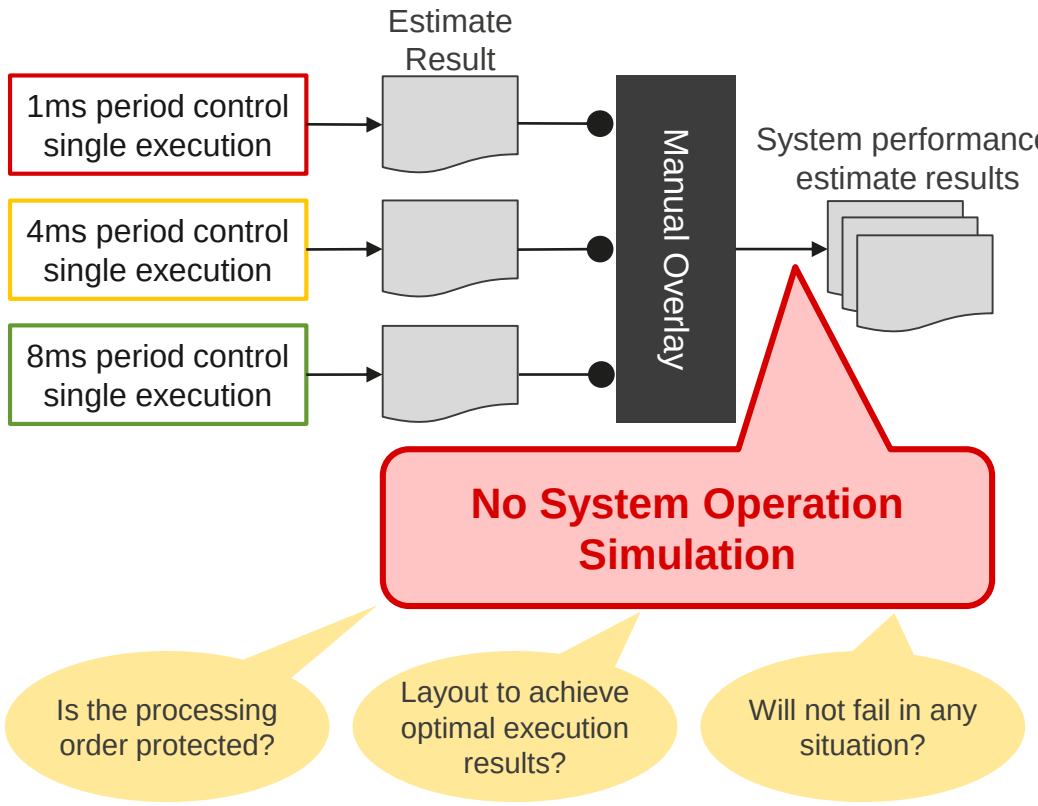


Image of Periodic Execution

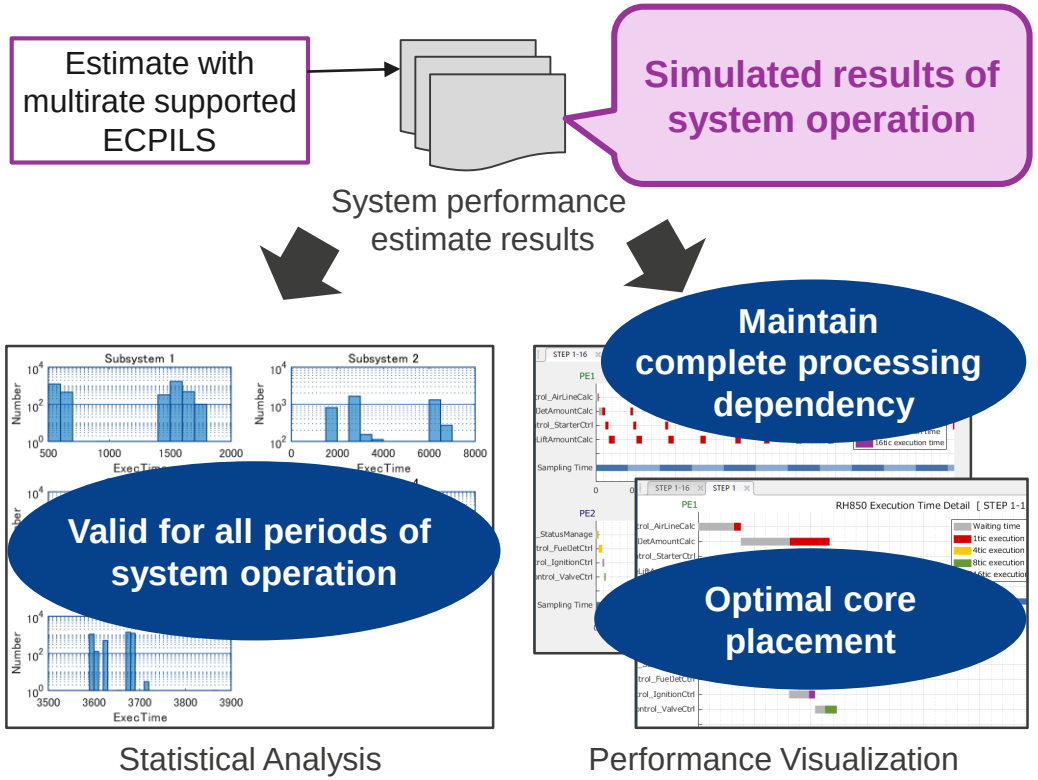
Enlarged image

MULTIRATE CONTROL SYSTEM VERIFICATION NOW POSSIBLE

Up to now:
lack of validity when the entire system was operated



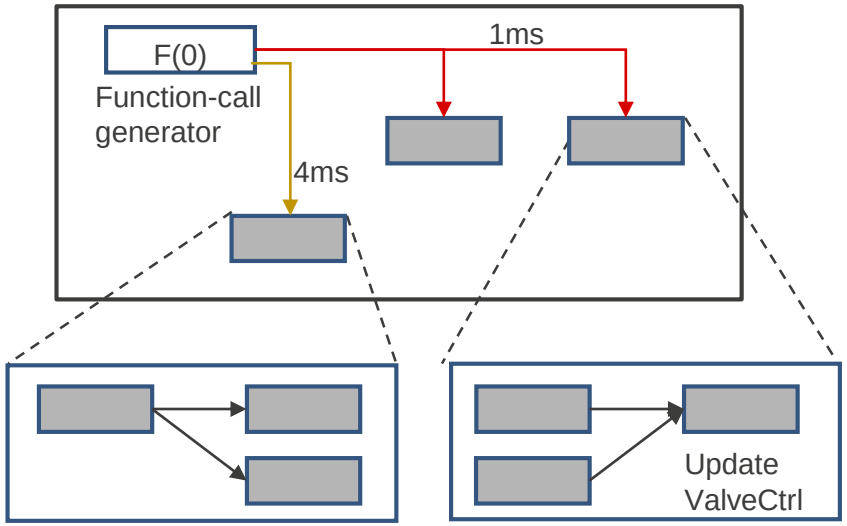
Overall system can be estimated and verified by simulation



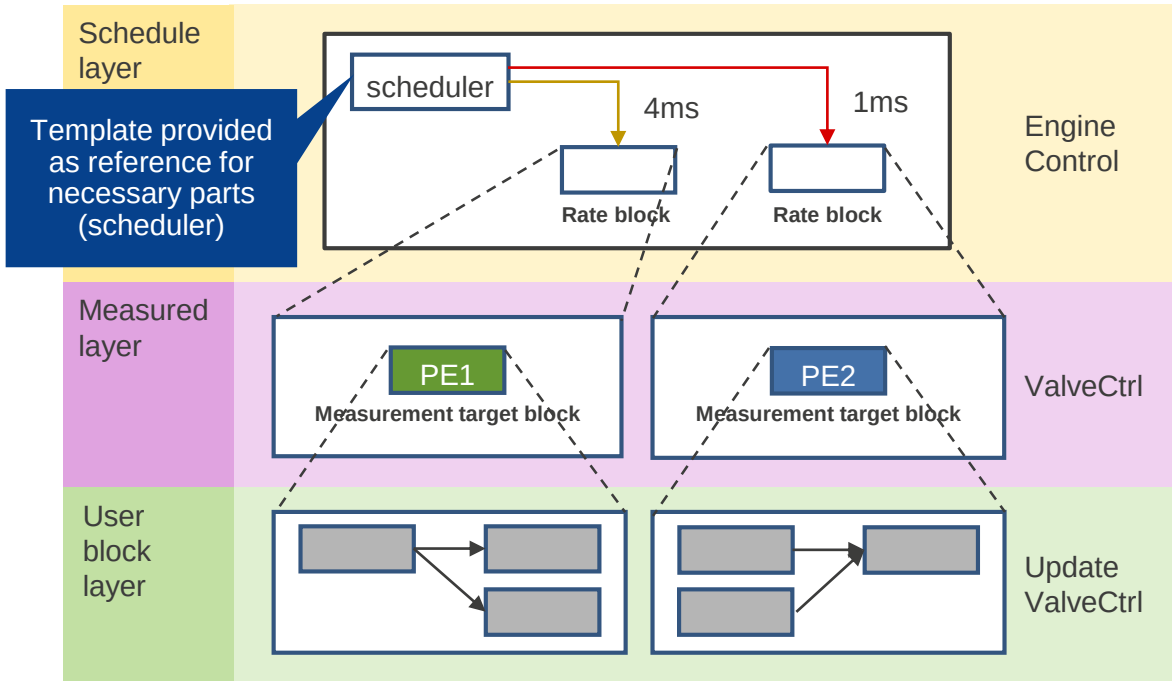
CONFORMS TO JMAAB CONTROL MODELING GUIDELINES FOR MODEL-BASED DEVELOPMENT

Existing customer assets (multirate model) can easily be applied in a format conforming to JMAAB control algorithm modeling guideline

- Example of standard Simulink multirate model configuration



- Example of ECPILS-RH multirate model configuration

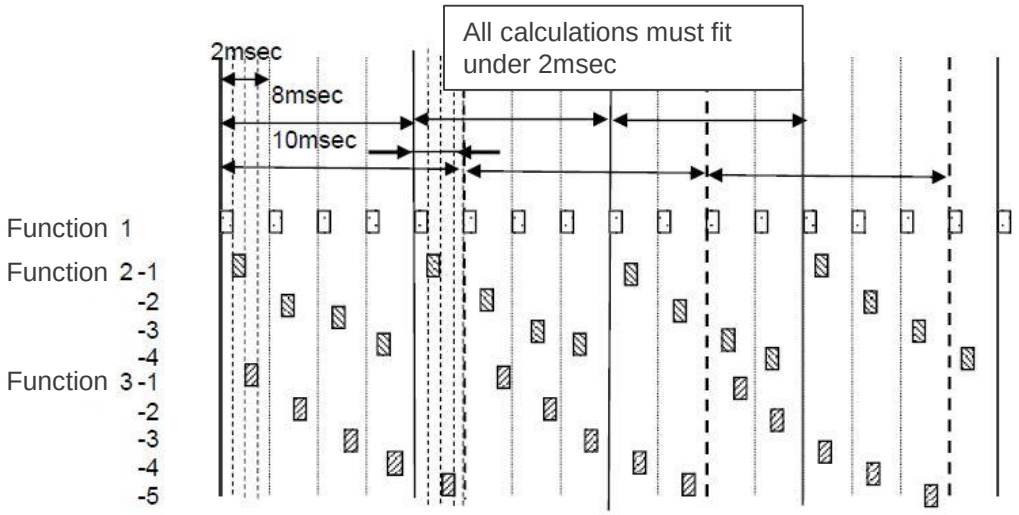


REFERENCE: JMAAB CONTROL MODELING GUIDELINE MULTIRATE CONTROL MODELING WITH ECPISL-RH ASSUMPTION

Following the JMAAB control modeling guideline recommendations, generate code using the **multirate-single task method** with control model type α (**using schedule layer**) as an assumption.

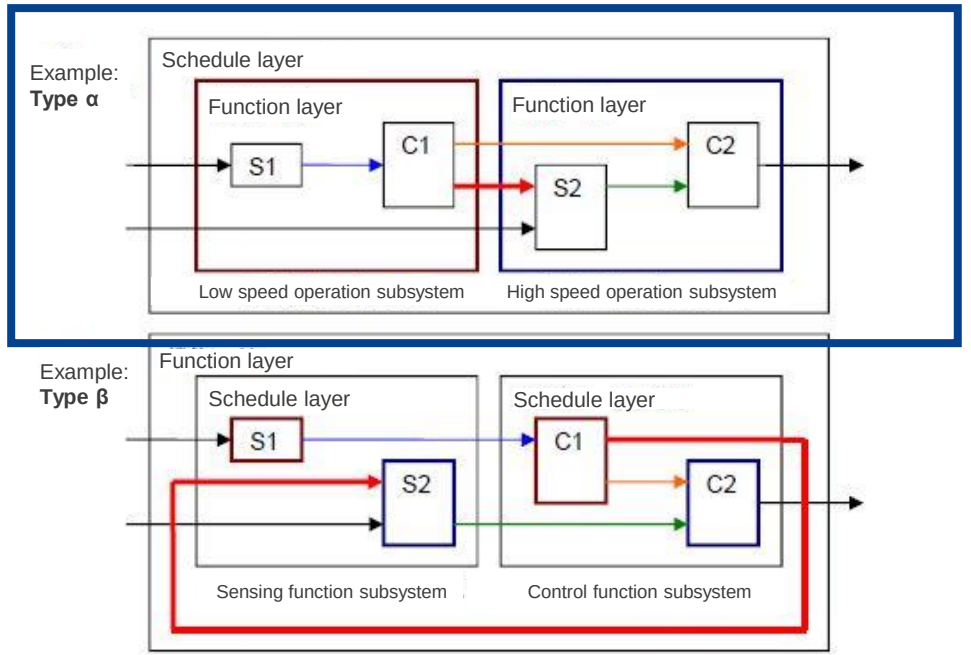
Example image of multirate-single task method

*Reference: JMAAB Guideline



J control model type α

*Reference: JMAAB Guideline



ROADMAP

ROADMAP OF EMBEDDED TARGET FOR RH850 MULTICORE

Embedded Target for RH850 Multicore V4.03

- Automatic parallelization
- Multicore code generation
- Performance analysis of each block
- User designated core assignment
- Single rate model support
- Singlecore / Multicore support

- C1H
- E1M-S
- E1M-S2
- F1L
- F1H
- F1K
- F1KM

<NEW> Embedded Target for RH850 Multicore V5.00

* Scheduled in FY2018, Fall

- **Multirate model support**
- Add any device

- **P1H-C**
- **P1M-C**
- C1H
- E1M-S
- E1M-S2
- F1L
- F1H
- F1K
- F1KM

Continuous enhancement

- Usability enhancement
- E2X-FCC2 (under development)
- RX, R-CAR (under planning)

Addition of new functions (under R&D)

- Support other model architecture
- Support RTOS/BSW
- Verification of parallel operation

Renesas.com