Background Multi-Rate LMS Calibration Circuit for 15MHz-BW 74dB-DR CT 2-2 MASH ΔΣ ADC in 28 nm CMOS

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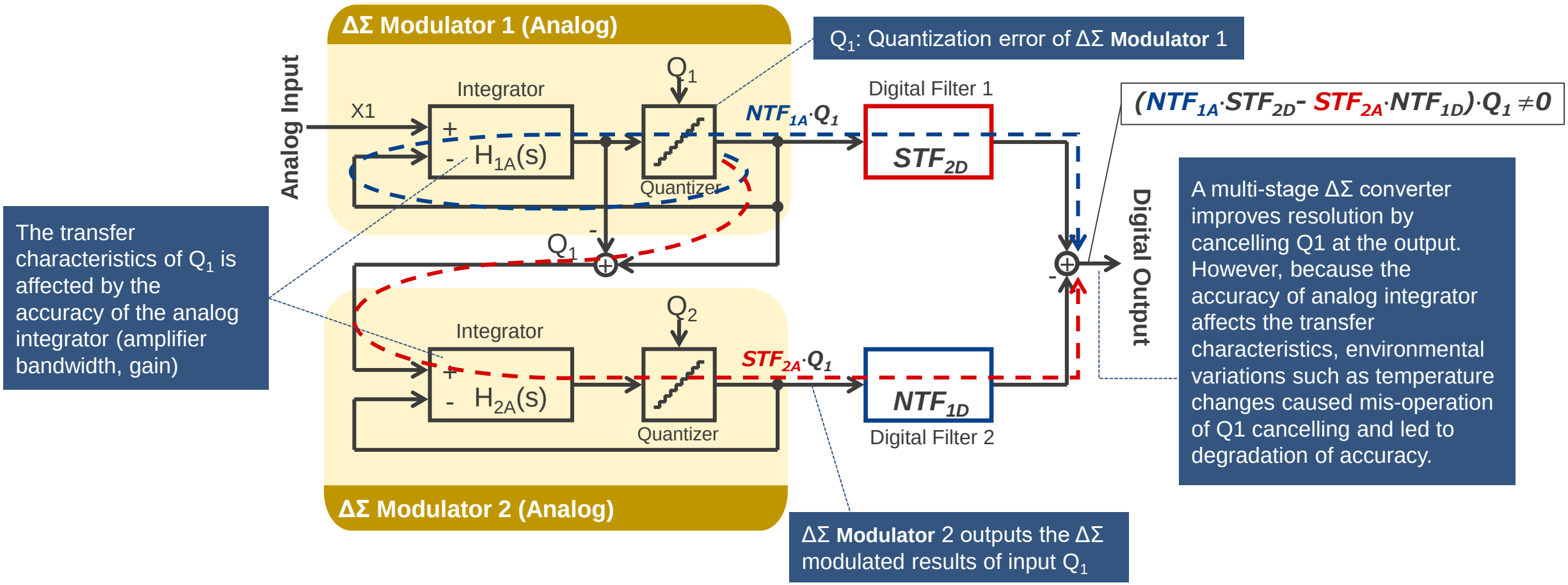
RENESAS ELECTRONICS CORPORATION

ISSUES OF CONVENTIONAL MULTI-STAGE ΔΣ CONVERTER

A multi-stage ΔΣ converter is extremely stable against excessive input, but has issues achieving higher precision.



NEW TECHNOLOGY DESCRIPTION

(1) Technology using LMS algorithm to measure and calibrate the transfer function of a continuous-time ΔΣ modulator

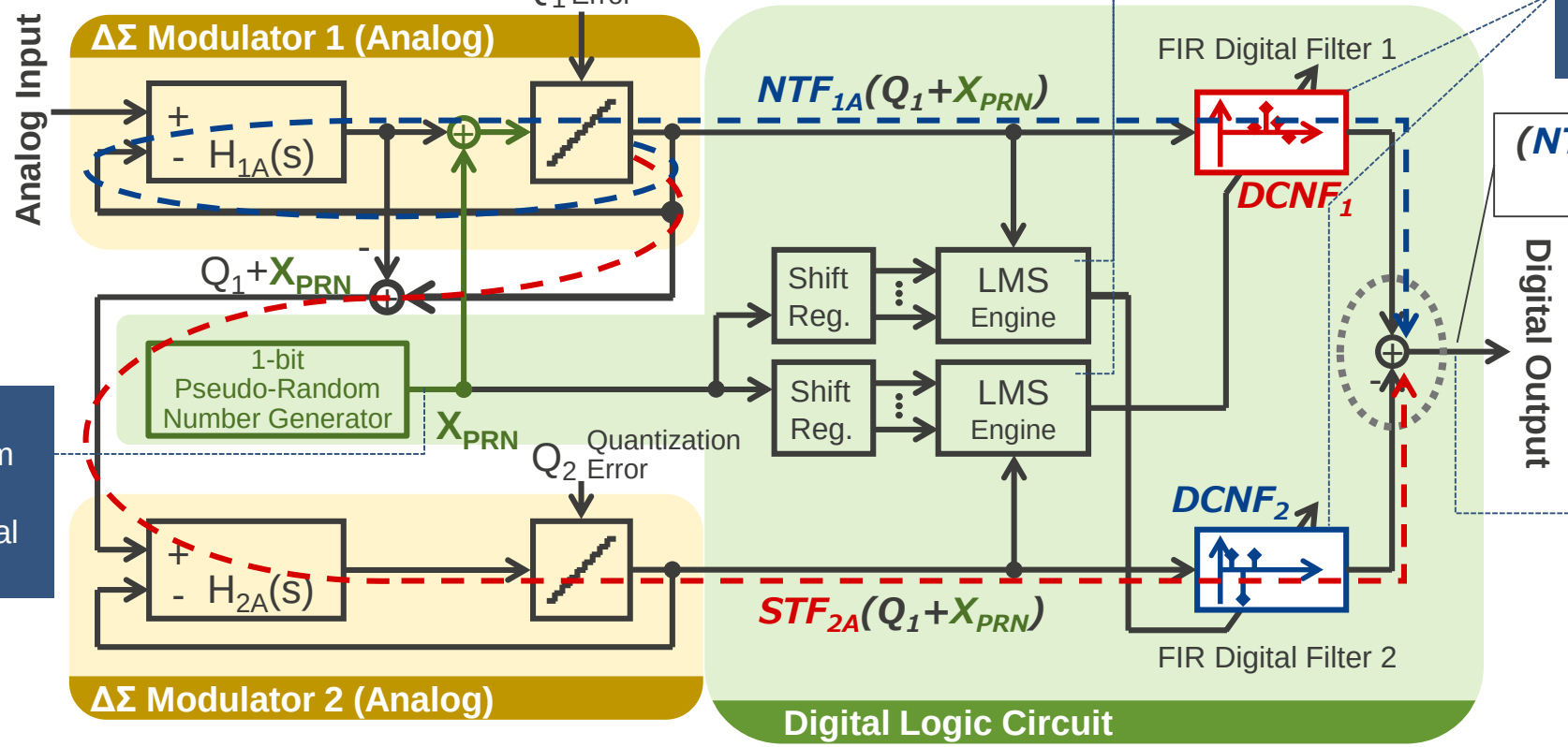
To enhance precision of a multi-stage ΔΣ converter, a new circuit technology is developed to enable background digital calibration.

(2) Searches Q_1's transfer function in real-time by using two LMS (least mean square) engines

(3) Reflects coefficient search results to the coefficient of FIR digital filter

$$(NTF_{1A} \cdot DCNF_1 - STF_{2A} \cdot DCNF_2) \cdot (Q_1 + X_{PRN}) = 0$$

(1) Inputs 1-bit pseudo-random number as a reference signal for calibration



(4) Calibrates analog accuracy in the digital domain, and improves resolution by removing quantization error Q_1 and pseudo-random signal X_{PRN} on the output.
Background digital calibration improves stability against environmental variations, enables capable of achieving both robustness and high precision.

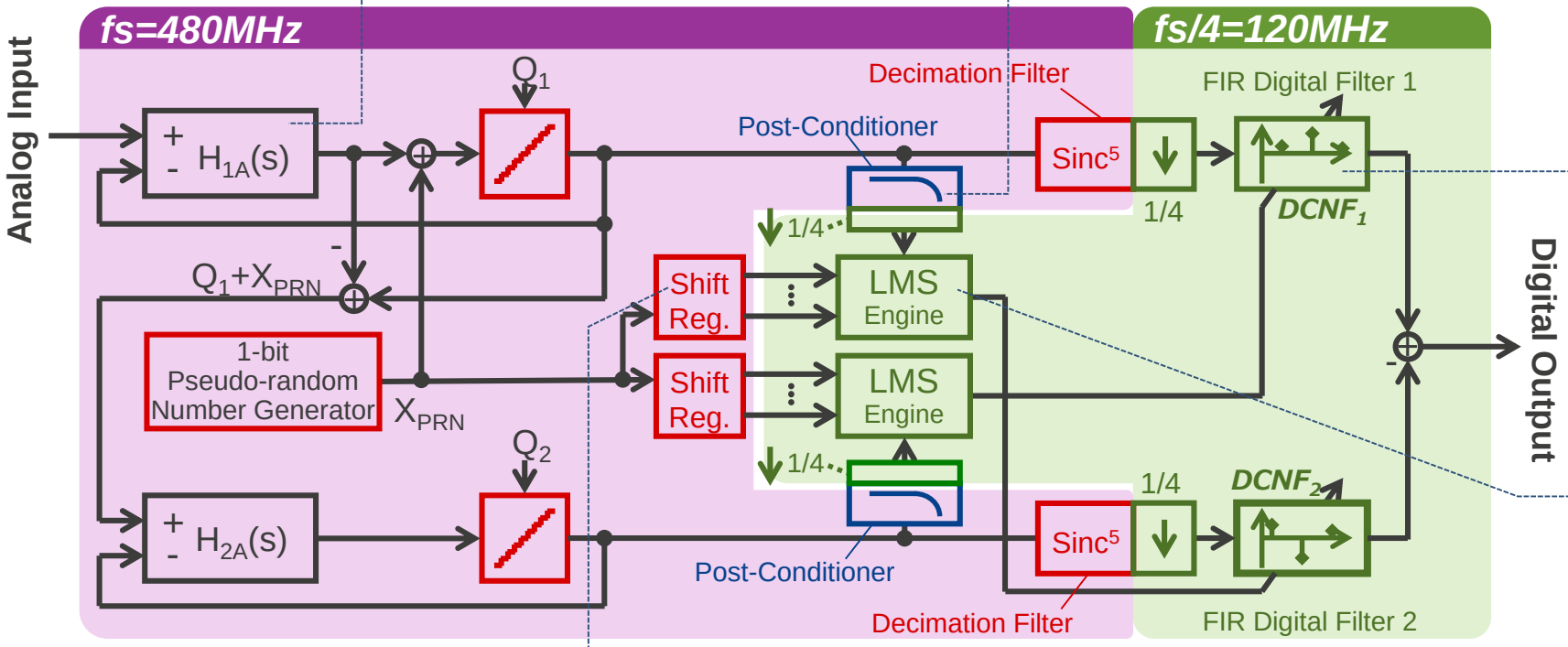
NEW TECHNOLOGY DESCRIPTION

(2) World's first multi-rate LMS search algorithm that enables smaller circuit scale and low power consumption

The issues of the LMS algorithm were the increasing operating current and logic scale. The post-conditioner enables the reduction of the number of taps for LMS engine and FIR filter, and also drastically lowers the operating frequency.

(1) If gain-bandwidth product of the integrator amplifier circuit is small, the transfer function will have a peaking

(2) Removes peaking and reduces the number of FIR filter taps



(5) Variable coefficient FIR filter computes signals with frequency rate reduced to one-fourth. A decimation filter is used for the rate reduction. Number of taps is drastically reduced from over 100 to 10.

(3) Data decimation is processed and LMS searching rate is reduced to one-fourth frequency.

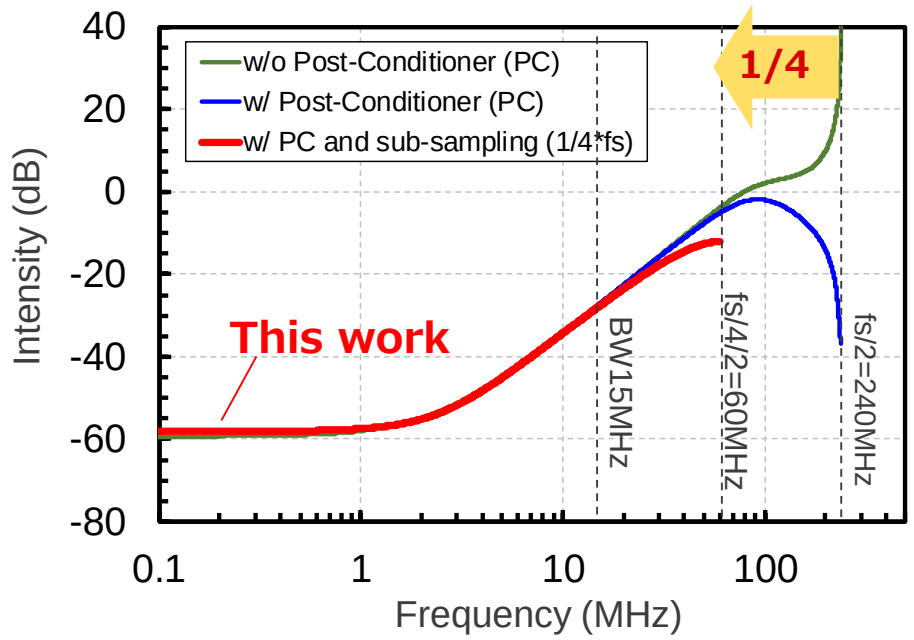
(4) Stores pseudo-random number data to deter effects of data decimation

NEW TECHNOLOGY DESCRIPTION

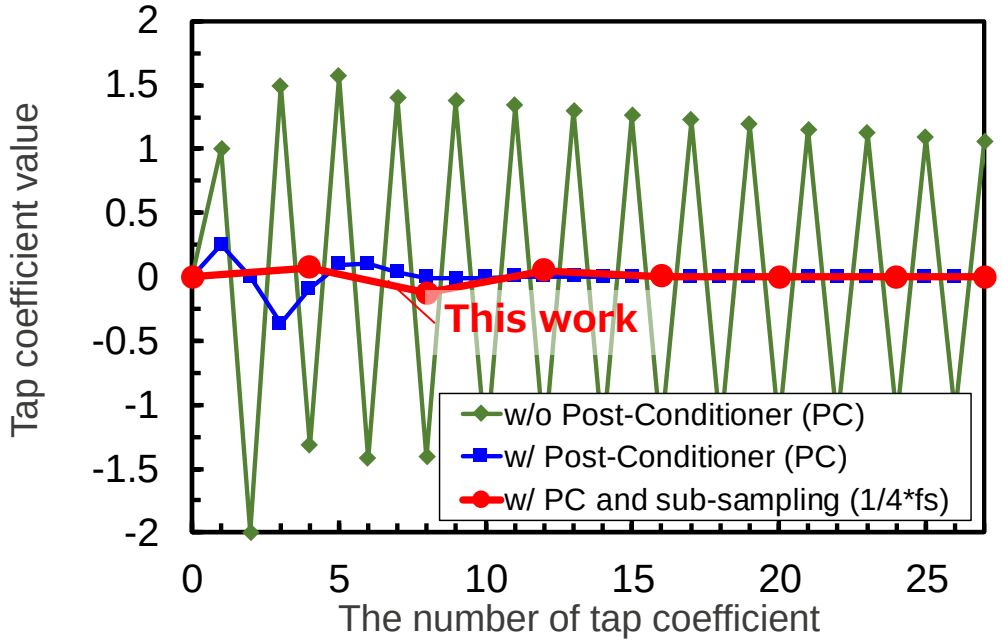
(2) World's first multi-rate LMS search algorithm that enables smaller circuit scale and low power consumption

This new technology enables the reduction of operating frequency (lower power) and a smaller number of digital filter taps (smaller logical scale).

Characteristics of Q_1 's noise transfer function frequency (NTF_{1A})



FIR filter degree (no. of coefficient) and coefficient value ($DCNF_2$)

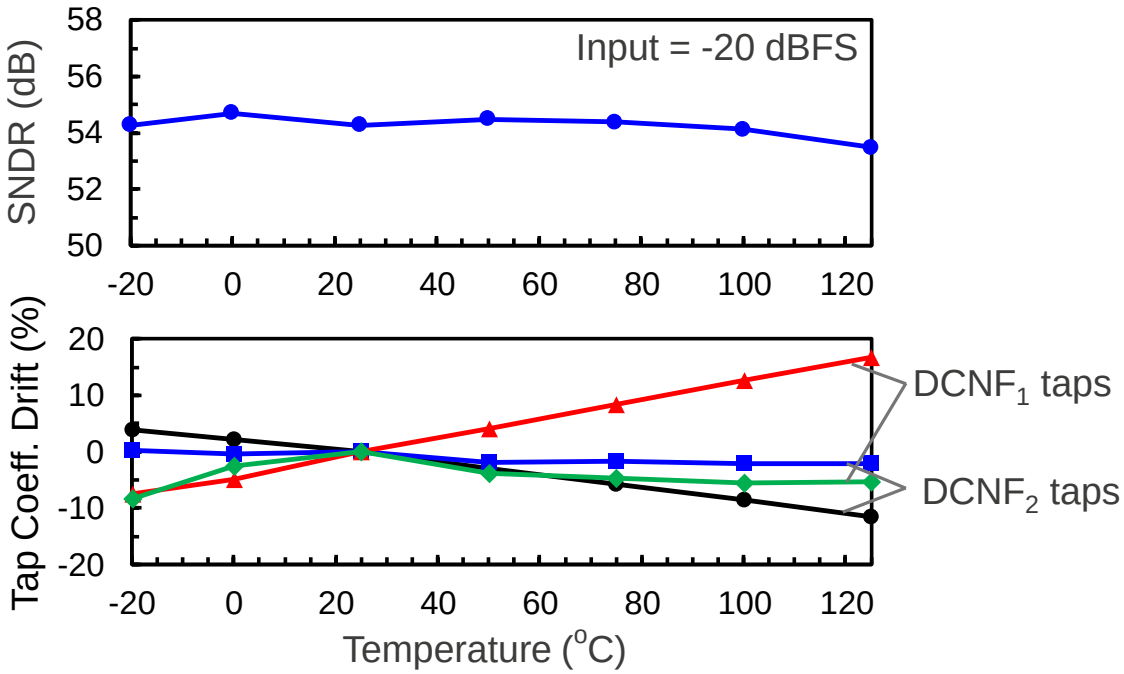


A post-conditioner enables removing peaking caused by lack of gain-bandwidth product for an amplifier circuit, and thus reduces the number of FIR filter taps from over 100 to 28. Also, by decimating the FIR filter operating frequency to one-fourth of the previous situation, the number of FIR filter taps can be reduced to 10.

TEST CHIP RESULTS

1. The test chip was fabricated in 28 nm process.
2. **Performance variations were held under 1dB** by optimally adjusting FIR digital filters against temperature changes.
3. After digital calibration, **achieved signal bandwidth of 15 MHz and dynamic range of 74.3 dB**

SNDR Temperature Dependency and FIR Filter Coefficient Value

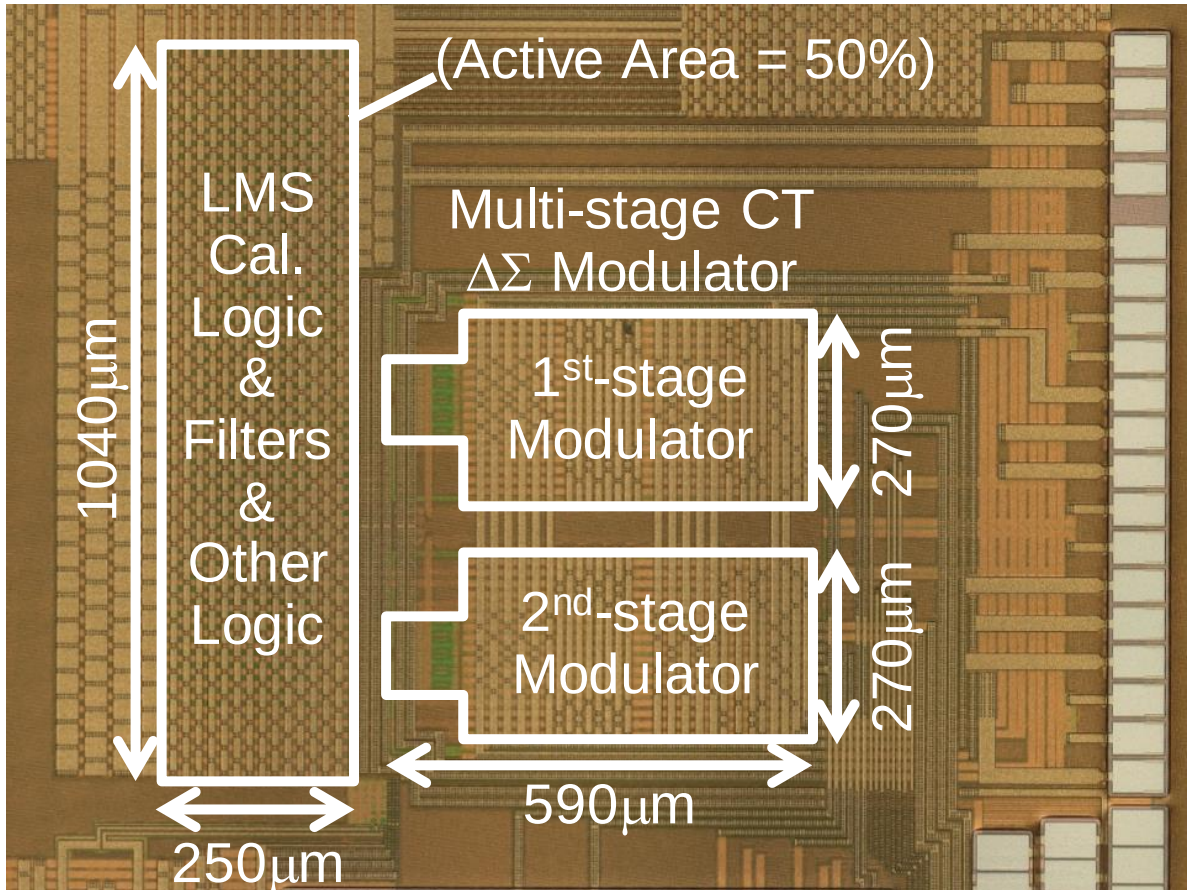


TEST CHIP PERFORMANCE SUMMARY

Test Chip Specifications

		This Result
Process (nm)		28
Oversampling Frequency (MHz)		480
Signal Bandwidth (MHz)		15
Dynamic Range (dB)		74.3
Power-supply Voltage	Analog (A)/ Digital (D)	1.1/1.0
Power (mW)	A / D	19 / 18
Area (mm^2)	A / D	0.28 / 0.13

Test Chip Photo



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