PRESENTATION HIGHLGHTS @ISSCC2021

ISSCC online QA session:
US PST: Feb 16, 8:30-9:30

TITLE :

A 12nm Autonomous Driving Processor with 60.4TOPS, 13.8TOPS/W CNN Executed by Task-separated ASIL D Control

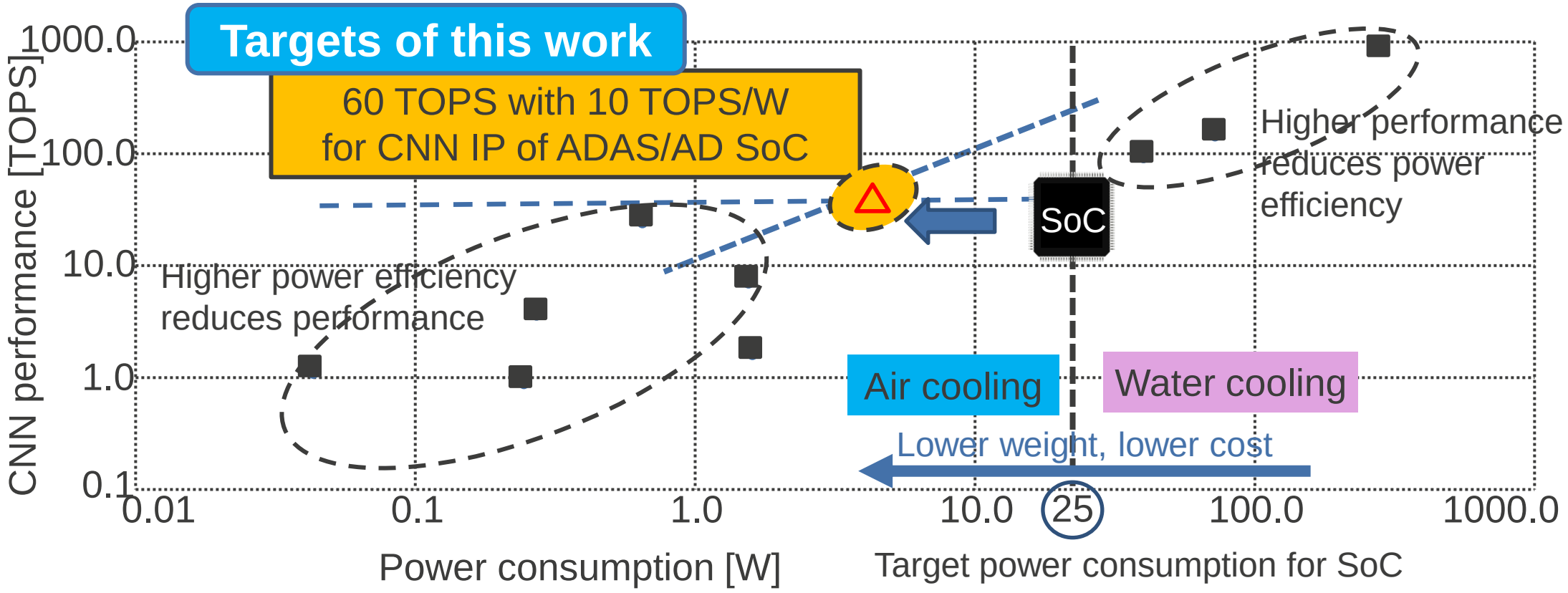
February 17, 2021
Automotive SoC Development Division
Automotive Solution Business Unit
Renesas Electronics Corporation

EXECUTIVE SUMMARY

- Renesas developed the processor technologies for automotive systems-on-chip (SoCs) used in applications such as advanced driver assistance systems (ADAS) and self-driving systems that aim to optimize both performance and power efficiency while supporting a high level of functional safety.
- The new technologies developed by Renesas and implemented in the R-Car V3U are described below.
  1. Development of high-performance CNN hardware accelerator with superior power efficiency
  2. Development of safety mechanisms for ASIL D systems capable of self-diagnosis
  3. Development of a support mechanism for freedom from interference (FFI) between software tasks
- Renesas presented these achievements at International Solid-State Circuits Conference 2021 (ISSCC 2021), which is taking place February 13 to 22, 2021.

BACKGROUND OF DEVELOPMENT (1)
MOTIVATION - CNN PERFORMANCE/WATT TARGETS

- Require optimization for both high DL performance and lower power efficiency
- CNN 60TOPS with 10 TOPS/W is the sweet spot for ADAS/AD systems



BACKGROUND OF DEVELOPMENT (2)

MOTIVATION - BENEFIT OF SOC W/ ASIL D* OFFERING

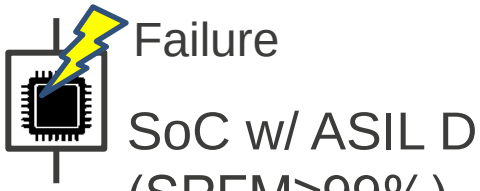
* Referring to process and metrics capabilities

SAE Level	Level 0	Level 1	Level 2	Level 3	Level 4	Level5
Assumed fault tolerance requiremen	Fail-Silent			Fault tolerance		
				Limited MRM	MRM	

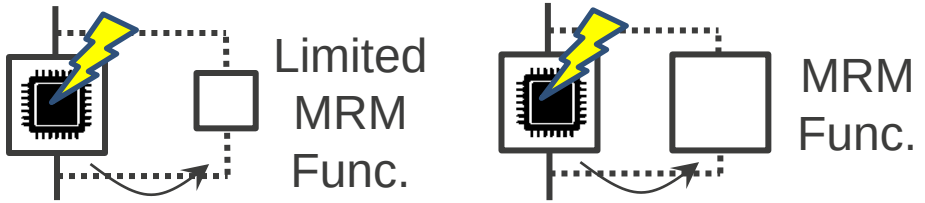
SoC w/ ASIL D

Target application of this work

Self-Diagnosis to enter fail-silent



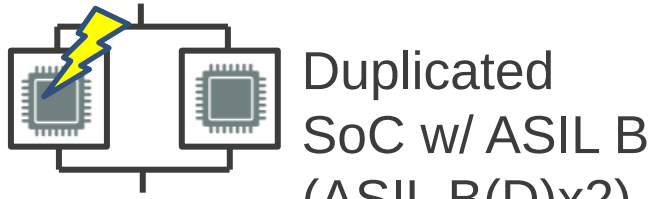
Self-Diagnosis to switch to the backup



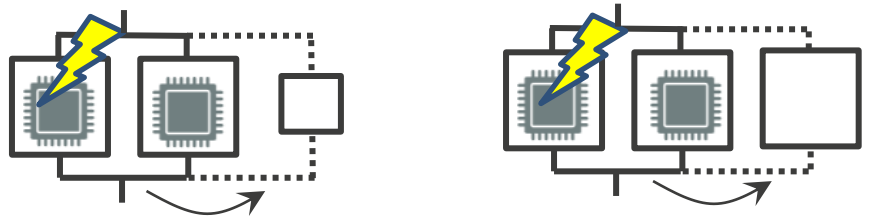
SoC w/less than ASIL D

- Higher BOM Cost
- Higher Complexity
- Higher Power

Comparing to enter fail-silent



Comparing to switch to the backup



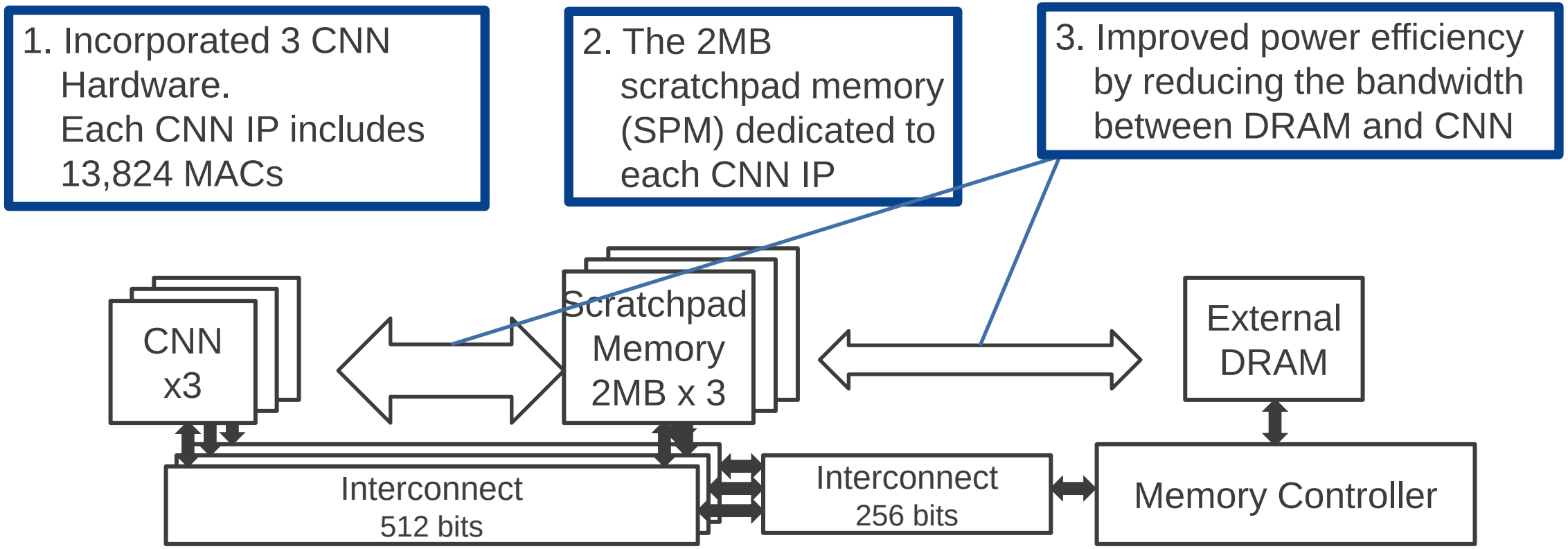
OVERVIEW @ ISSCC 2021

Renesas Develops Automotive SoC Technologies with CNN Accelerator Cores and ASIL D Control Combining World-Class Performance and Power Efficiency

1. Renesas has developed a convolutional neural network (CNN) hardware accelerator core that delivers a world-class combination of deep learning performance of 60.4 trillion operations per second (TOPS) and a power efficiency of 13.8 TOPS/W.
2. Renesas has developed sophisticated safety mechanisms for fast detecting and response of random hardware failures.
3. Renesas has developed a mechanism that allows software tasks with different safety levels to operate in parallel on SoC without interfering with each other.

DEVELOPED TECHNOLOGY 1
CNN HARDWARE WITH HIGH PERFORMANCE AND EFFICIENCY

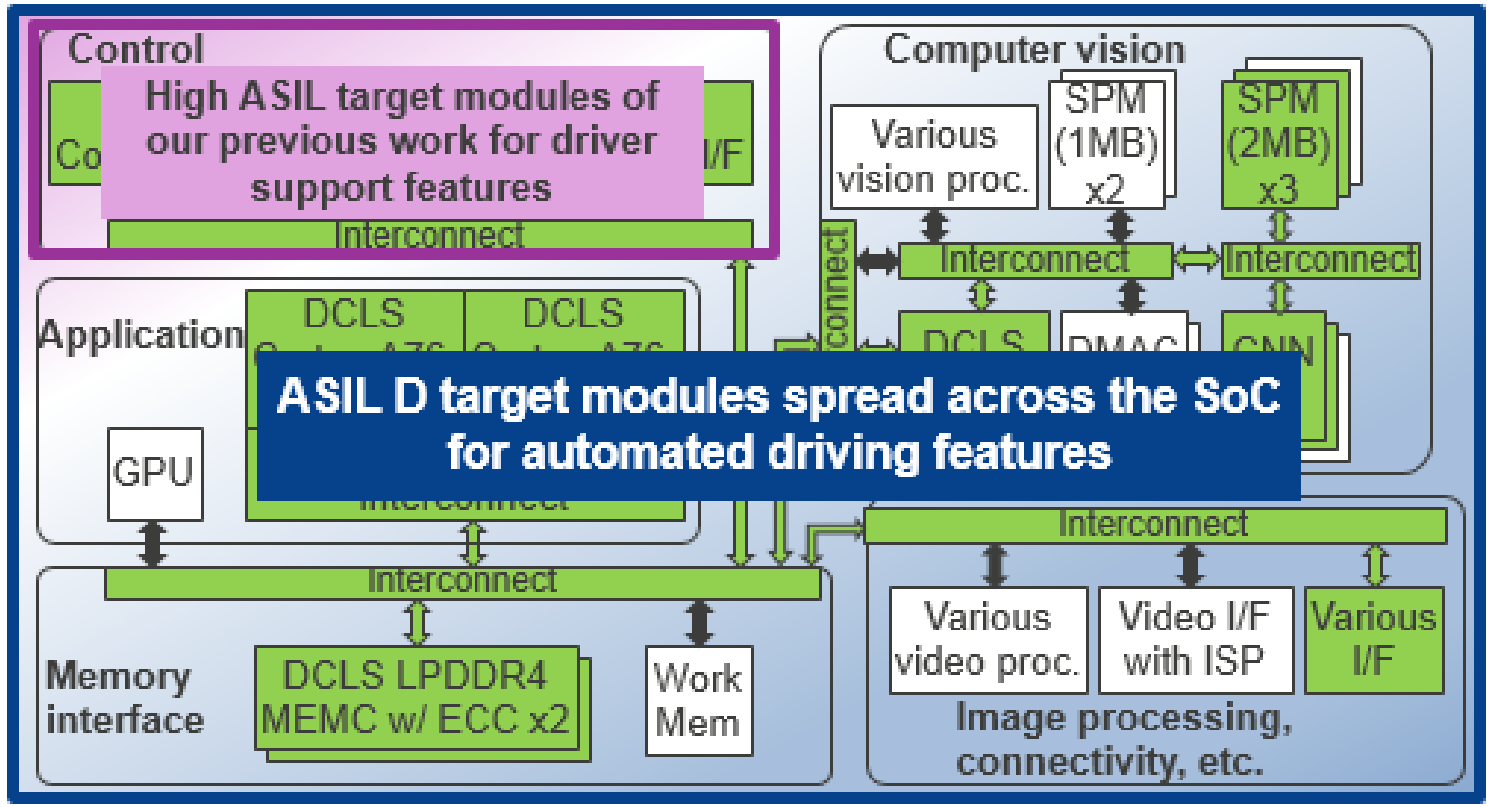
- Achieved performance 60 TOPS with efficiency of 10 TOPS/W



DEVELOPED TECHNOLOGY 2

SAFETY MECHANISMS CAPABLE OF SELF-DIAGNOSIS FOR ASIL D SYSTEMS

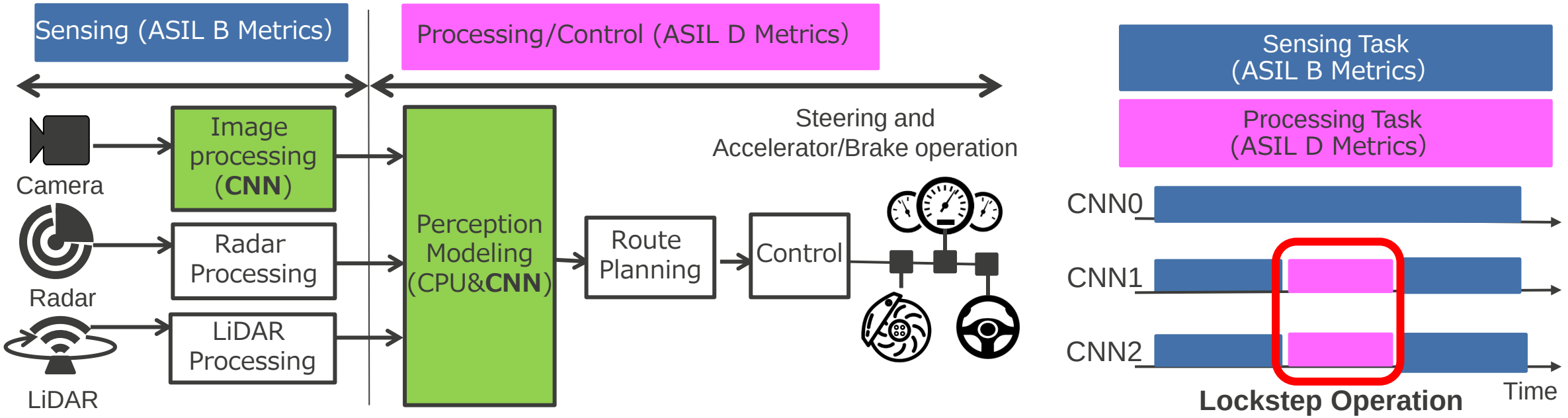
- Safety mechanisms for fast detecting and response of random hardware failures occurring in the SoC overall.
- Achieved both extremely high failure detection rate and reduced power consumption by combining safety mechanisms suited to specific target functions.



Green squares and arrows indicate ASIL D target module.

DEVELOPED TECHNOLOGY 2
SAFETY MECHANISMS FOR CNN ACCELERATOR

- The CNN accelerator is used for ASIL B image processing input from cameras and ASIL D perception modeling from the results input from each sensor.
- Most of the processing performed by the CNN accelerator is ASIL B image recognition processing.
- **Rather than configuring all CNN accelerators redundantly, only the ASIL D periphery perception modeling process is performed in lockstep operation to achieve ASIL D metrics with low power consumption.**

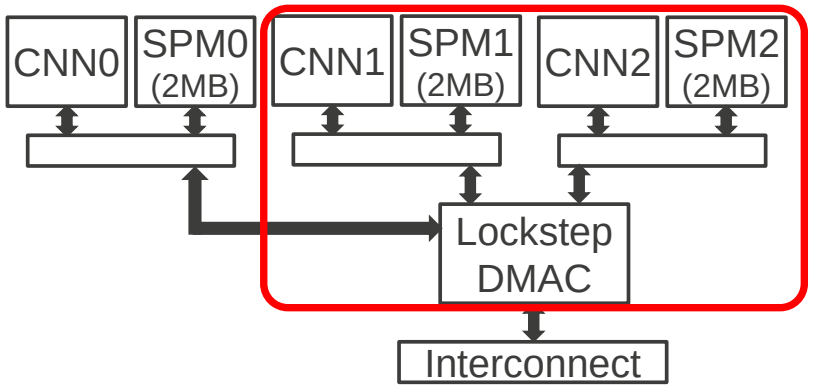


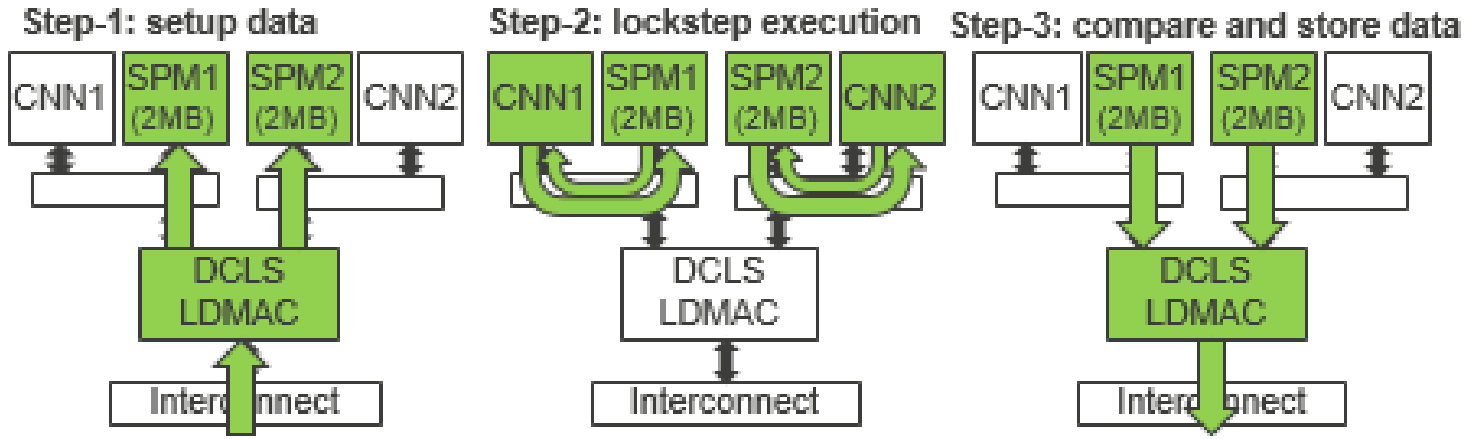
DEVELOPED TECHNOLOGY 2
HARDWARE SUPPORTED SOFTWARE LOCKSTEP

Implemented “Hardware Supported Software Lockstep" that can execute lockstep process for any period of time using CNN accelerator 1 (CNN1), CNN accelerator 2 (CNN2), and Lockstep DMAC.

Execute by 3 Step

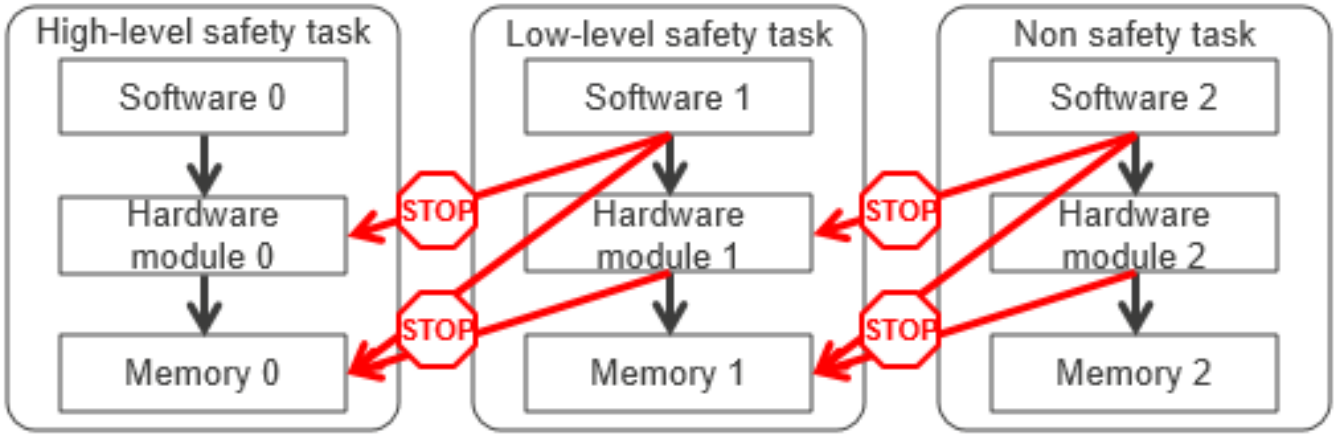
Step-1: LDMAC starts data transfer using the lockstep read descriptor.
=> LDMAC reads data from DRAM and stores in SPM1 and SPM2 both.
Step-2: CNN1 and CNN2 start the same operation.
Step-3: LDMAC stars data transfer using the lockstep write descriptor.
=> LDMAC compares with SPM2 data when transferring SPM1 data to DRAM.



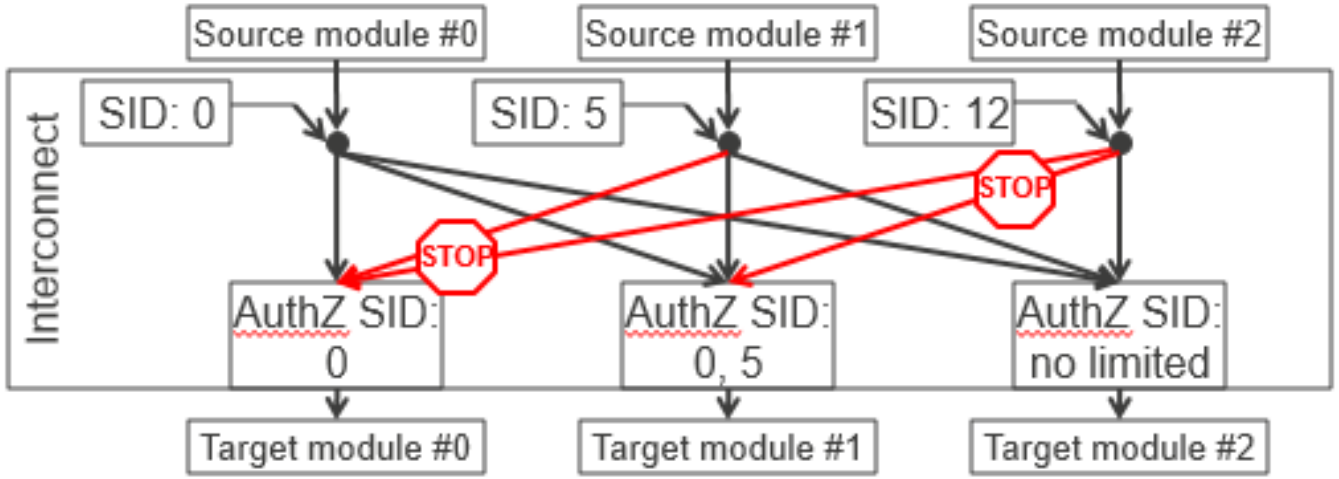


DEVELOPED TECHNOLOGY 3
SUPPORT MECHANISM FOR FREEDOM FROM INTERFERENCE (FFI)

Lower ASIL level tasks must not interfere with high-level safety tasks.

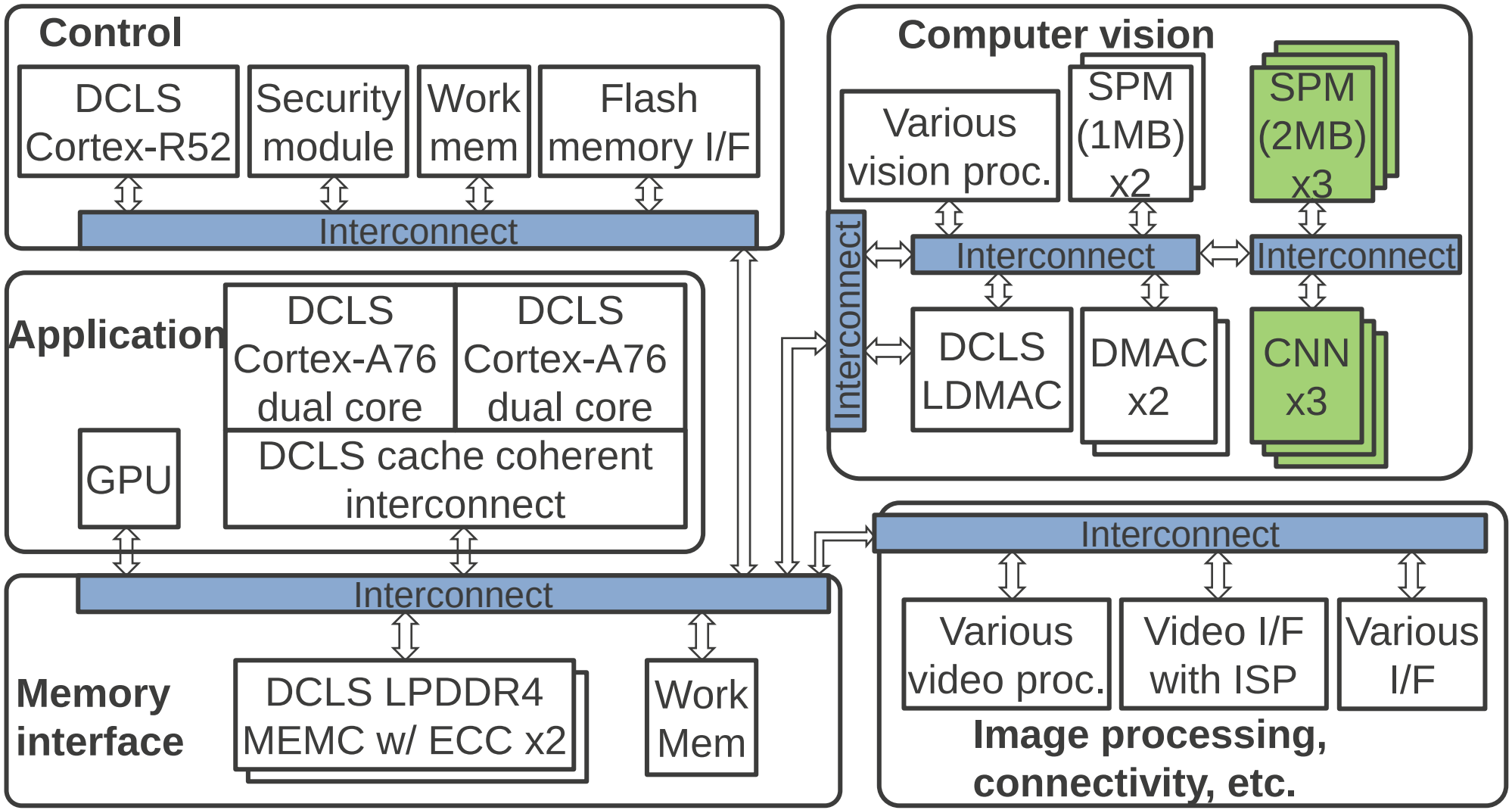


Support mechanism for Freedom From Interference(FEI) blocks unauthorized transactions and returned as the error response by monitoring all transactions in the interconnect of SoC

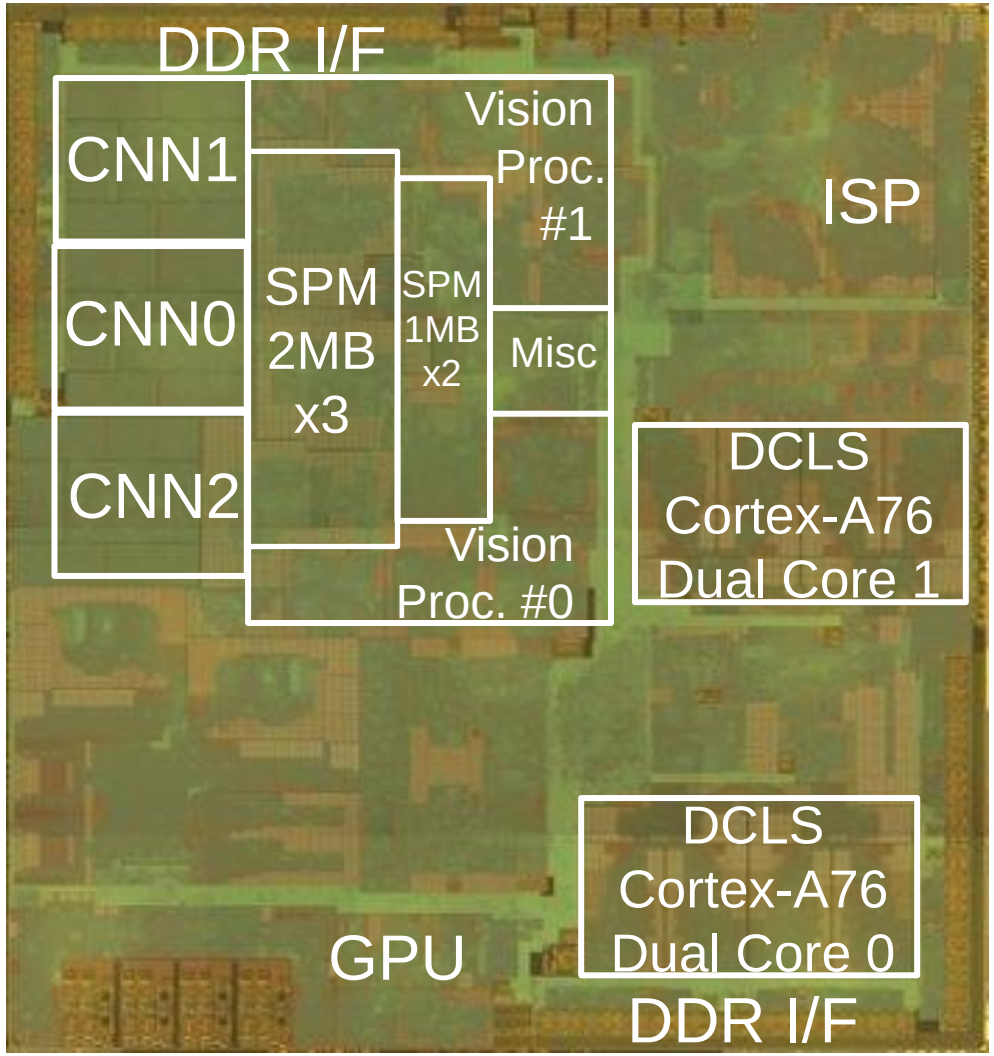


＊SID：Secure ID

Architecture Overview of R-Car V3U



R-Car V3U Overview



Process	12nm
Voltage	0.80V (Other than CPU and GPU) 0.85V (CPU,GPU)
Chip size	230.46mm^2
On chip SRAM	~ 41.6MB
Performance	1.8GHz Dual core lockstep (DCLS) ARM Cortex-A76 dual core x2 1GHz DCLS safety processor LPDDR4-4266 16bit x8 600MHz GP-GPU
Key accelerators	Theoretical maximum 66TOPS CNN hardware 480Mpixel ISP x4, Image classification x8
High speed interfaces	PCIe Gen4 x4, Gbit-EtherAVB x6 MIPI CSI-2 10Gbps x4, DSI 10Gbps x4
Functional safety	Process: ASIL D Metrics: SPFM≥99%/LFM≥90% enabled through on-chip measures allowing fast system fault tolerant time interval

<APPENDIX>
SAFETY MECHANISM FOR ASIL D TARGET

Domain	ASIL D Target Module	Applied Safety Mechanism
Control	Cortex-R52, Security module, Work mem, Flash memory I/F	Dual core lockstep, ECC/EDC, End-to-end protection
Memory	LPDDR4 memory controller	Dual core lockstep, ECC/EDC
Application	Cortex-A76, Cache coherent interconnect	Dual core lockstep, ECC/EDC
Computer vision	CNN, LDMAC, SPM(2MB)	Dual core lockstep, ECC/EDC, Hardware Supported Software Lockstep, Runtime test
Connectivity	PCIe, EAVB, CAN-FD, Flexray	End-to-end protection
Interconnect	All modules	End-to-end protection, Dual core lockstep, ECC/EDC